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Research on Techniques for Enhancing the Speed of Low-Power Operational Amplifier

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Abstract:

In the context of low utilization, this paper explores various techniques for enhancing the speed of operational amplifier (OA). The main text delves into three methods to gain equilibrium: fully differential operational amplifier (FDA), two-stage operational transconductance amplifier (OTA), and a novel high-speed calculation system architecture employing a "rhombus crystal tube." The FDA improves speed by minimizing noise and enhancing bandwidth and output voltage swing, without increasing power consumption. The design of the two-stage OTA combines the characteristics of a differential amplifier and a telescopic amplifier, optimizing gain and slew rate through Miller compensation and noise gain manipulation, thereby achieving high-speed performance. A novel high-speed operational amplifier structure employs diamond transistors to supply substantial current for capacitor charging, enhancing the slew rate and overall speed. Throughout the text, these methods are presented as a means to jointly promote high speed, low power consumption, and the handling of a significant number of transistors. To further increase the speed, the size of the microcrystalline tube is crucial. The research direction is outlined, and while the design equipment is in the foreground, there remains room for progress, especially in applications for large-scale electrical models. Future research aims to enhance the power efficiency of circuits, making them more practical and efficient. This study provides valuable insights into balancing power consumption and speed in advanced electronic devices.

Keywords: low power consumption; high speed; operational amplifier.

1. Introduction

Analog circuits are an indispensable part of electronic circuits, playing a crucial role across various societal domains with strong practical utility. Analog circuits refer to the type of circuits used for the transmission and processing of analog signals, and they are widely utilized in daily life. For instance, commonly encountered devices such as low-frequency amplifiers and FM radios rely on the support of analog circuits for their operation. From various perspectives, the characteristics of their applications can be analyzed as follows: Firstly, the function values of analog circuits are infinite. Secondly, when the image information changes, the signal waveform is correspondingly affected and altered. Analog signals are manifested within waveforms, exhibiting a characteristic of continuity, which makes them less susceptible to interference [1].

OAs are fundamental components in analog circuitry and are widely utilized in a variety of mixed-signal processing applications, including analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, and switched-capacitor circuits [2]. With the rapid development of information technology, there are increasingly higher demands for the power consumption and speed of OA. Enhancing the speed of OA while reducing its power consumption can meet the requirements of more precise electronic devices. However, low power consumption and high speed present a paradox. Reducing power consumption often results in a decrease in speed, whereas increasing speed typically comes at the expense of higher power consumption [3]. Therefore, enhancing the speed of OA while maintaining low power consumption is a crucial topic. Most high-speed OAs are built using complementary bipolar transistors. To enhance the speed of these OAs, key design and technological strategies include minimizing the parasitic capacitance of the collector, which can be achieved through dielectric isolation of the integrated components, such as silicon-on-insulator (SOI) technology. Additionally, increasing the cutoff frequency of these transistors is accomplished by reducing the size of the emitter region and thinning the active base. The incorporation of SiGe-SOI structures is also employed to further improve performance [4].

This paper discusses techniques for enhancing the speed of low-power OA and proposes three methods to achieve this goal. The first method involves the use of FDA,

which can mitigate the impact of noise, increase bandwidth, enhance output voltage swing, and improve speed, while maintaining and even enhancing the original performance of the OA. The second method is the two-stage OTA, which is an incremental improvement based on the differential amplifier and telescopic amplifier, combining the advantages of both to ultimately achieve high-speed operation in a low-power context. The third method is the novel "diamond transistor" structure high-speed OA. Unlike the first two methods, this approach achieves high-speed operation by modifying the transistor structure and current sources rather than altering the circuit configuration. Therefore, this third method can be combined with the first and second methods to further enhance the speed of OA.

The first chapter of the paper serves as an introduction, providing an overview of analog circuits, OA, and the research background and significance of low-power high-speed technology. The second chapter presents the main content of the research, analyzing three techniques for enhancing the speed of low-power OAs: FDA, two-stage OTA, and the novel "diamond transistor" structure high-speed OA. The final chapter concludes the paper with a summary of the findings.

2. Techniques for Enhancing the Speed of Low-Power OA

2.1 FDA

With the advancement of deep submicron processes, the channel lengths of transistors have become increasingly smaller, leading to a significant increase in the intrinsic speed of MOSFETs [5]. The characteristic frequency f_T of a MOSFET is defined as the frequency at which the small-signal current gain of the device falls to unity, assuming the source and drain terminals are AC grounded [6]. This can be expressed by the following equation (1):

$$f_T = \frac{3 \bullet \mu}{4\pi \bullet C_{ox} L^2} (V_{GS} - V_{TH}) \tag{1}$$

From this, we can deduce that reducing the channel length L and increasing V_{GS} can enhance f_T, resulting in a smaller period. Therefore, to achieve higher-speed OAs, selecting the minimum channel length is advantageous. The reduction in channel length also leads to a decrease in dynamic power consumption [7]. This relationship can be described by equation (2):

$$P_{dynamic} = \alpha \bullet C \bullet V^2 \bullet f \tag{2}$$

However, this reduction in power consumption comes at the expense of the OA's performance. As indicated by the equation $g_m r_0 \propto \sqrt{L}$, the gain of the OA decreases with the reduction in channel length. To achieve a low-power OA with enhanced speed without compromising performance, we can employ FDA.

FDA offers several advantages: it is less susceptible to common-mode noise, eliminate the mirror pole, which significantly affects the bandwidth and stability of high-speed OAs, and thus allow for larger bandwidth, higher speed, and greater output voltage swing. Additionally, even-order nonlinearities do not appear in the differential output of balanced circuits [8].

In FDA, two matched feedback networks and a common-mode feedback circuit are required to control the common-mode output voltage. This necessity arises because achieving a balance between the p-type and n-type current sources in high-gain differential amplifiers is not feasible [9].

Based on the above analysis, we can preliminarily determine the main structure of the high-speed OA in this design, which includes the input stage, output stage, biasing circuit stage, common-mode feedback circuit stage, and frequency compensation circuit stage [5]. The overall structure is shown in Fig. 1.

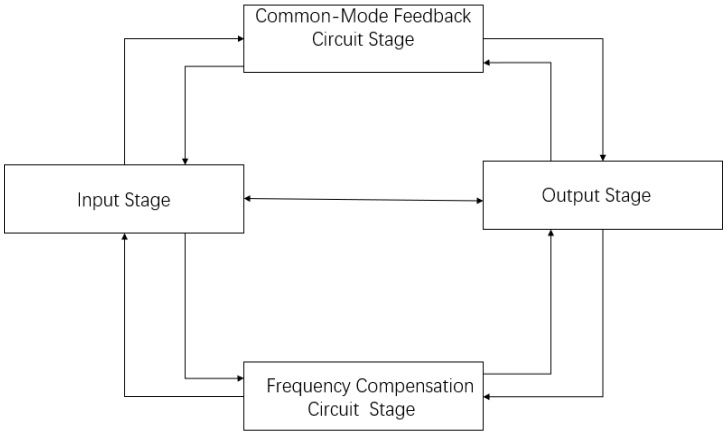

Fig. 1 Overall Structure Diagram of High-Speed OA

2.2 2-Stage OTA

High-speed OTAs are advantageous for driving high capacitive loads in comparison to standard amplifiers. The rapid response of these high-speed OTAs shortens the capacitor's charging time. Consequently, despite a slight reduction in gain, the output can still be effectively amplified and sent to an ADC converter or signal block driver with minimal delay. [10].

Formula (3) presents the general equation for calculating the slew rate. In this equation, I_0 represents the output current, and C refers to the capacitance at the amplifier's output. Increasing the circuit's current enhances the slew rate. To maintain the same gain without altering the overdrive voltages of the MOSFETs, the transconductance g_m must be adjusted. Reducing the transistor aspect ratio decreases the overall size of the MOSFET. This enables high-speed operation and, in turn, increases the slew rate [11].

$$SR = \frac{I_0}{C} \tag{3}$$

2.2.1 Differential Amplifier

Fig. 2 displays the corresponding schematic that has been designed. A differential amplifier generally includes a pair of transistors, which can be either bipolar junction transistors (BJTs) or metal-oxide-semiconductor field-effect transistors (MOSFETs). It functions with two inputs, labeled as inverting and non-inverting, and collects an output that is corresponding to the voltage distinct from these inputs [12].

The equation (4) provides the gain of the differential amplifier. The overall transconductance is referred to g_{m1}.

The output transconductance can be calculated by applying a test voltage at the output and determining the resulting output transconductance. The overall amplifier gain is expressed by Equation (5).

$$Gain = G_m \bullet R_{OUT} \tag{4}$$

$$A_d = \frac{g_{m1}}{g_{ds2} + g_{ds4}} \tag{5}$$

The main purpose is to amplify the difference between the two input signals while minimizing any signals that are common to both inputs. A high Common-Mode Rejection Ratio (CMRR) is preferable because it signifies the amplifier's capability to reject common-mode signals, thus improving the differential gain.

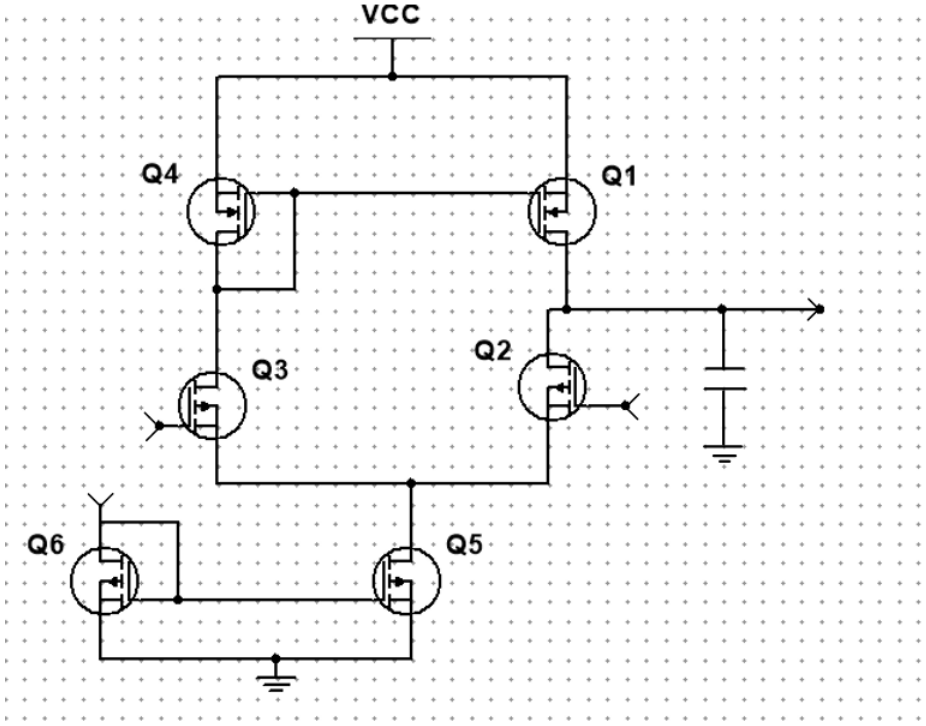

Fig. 2 Differential Amplifier Schematic

2.2.2 Telescopic Amplifier

To improve the gain value and slew rate of a telescopic amplifier, four additional transistors are incorporated as cascode transistors. This cascode configuration enhances the output resistance, thereby increasing the gain. Fig. 3 shows the schematic.

Telescopic amplifier is dispayed in Fig. 3, specially boasting advanced frequency capabilities and lower energy consumption compared to initial topologies. The entirety of transistors in this configuration performance in the saturation region. To achieve ideal attenuation of common mode signals, frequency range, and gain, it is crucial that transistors Q1 and Q4, Q2-Q3, and the tail current source Q5 are appropriately designed. When the input ranges from 1.1V to 1.4V, the output swing is approximately 0.8V. This composition offers a scaling ratio that is twice that of a flip-flop sense amplifier. The author introduces a schematic that leverages the high-speed benefits of the telescopic design [13].

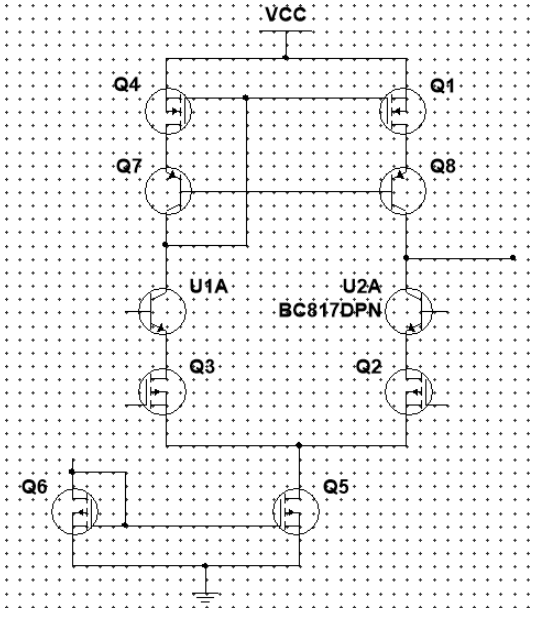

Fig. 3 Telescopic Amplifier Schematic

2.2.3 2-Stage OTA

Through the analysis of the above two types of OAs, their advantages and disadvantages can be integrated to improve and develop a two-stage OTA. The schematic of the two-stage OTA is shown in Fig. 4.

A 2-stage configuration is selected, with the last stage operating as a follower of source. To ensure stability, a compensation capacitor is employed between the stages as Miller compensation. To achieve sufficient gain and a higher slew rate, the current supply is boosted, which is compared to alternative designs [10]. Negative feedback loop with resistors acts as a voltage partitioner. To maintain durability, signal-to-noise ratio improvement is applied to enhance gain and preserve the reaction loop, despite the increase in noise. A 10fF compensation capacitor is utilized between the stages for Miller compensation [14]. Stability is achieved by adjusting the noise gain, increasing it while maintaining signal gain. This reduces the corner frequency, ensuring stability at the expense of a lower corner frequency. A one stage telescopic amplifier is inadequate for driving resistive loads independently, as the majority of the current passes through the resistors, leaving limited current for the equivalent capacitance. By adding a small integrating capacitor to establish a minor feedback connection between the second and first stages, the input terminal remains at a low voltage, lowering the current going through the output resistance of the initial stage.

Stability is preserved through noise-gain manipulation, which increases gain of noise excluding impacting the gain of signal. This approach reduces the unity gain frequency, thus achieving stability to the sacrifice of a decreased unity corner frequency.

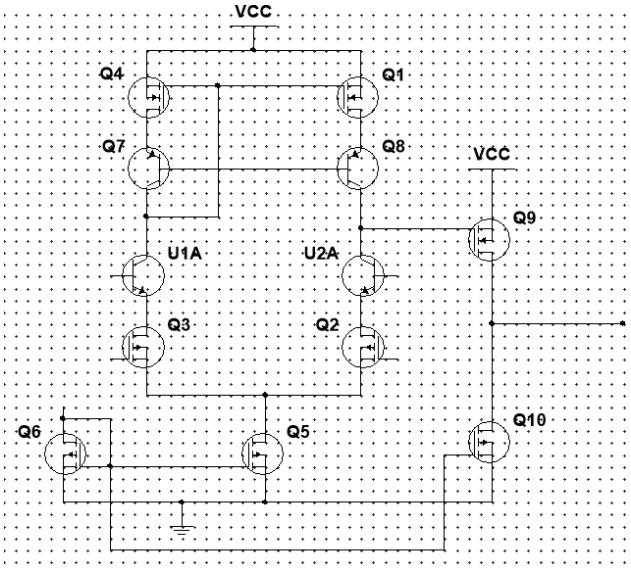

Fig. 4 2-Stage OTA Schematic

2.3 A Novel "Diamond Transistor" Structure For High-Speed OA

Fig. 5 illustrates the main schematic of OA[15]. The input stage mainly comprises a pair of "diamond transistors" (Q1, Q2, Q4, Q5 and Q8, Q9, Q12, Q13), where Q4, Q5 and Q12, Q13 are biased by Q1, Q2 and Q8, Q9 respectively in the form of source followers. Additionally, the circuit incorporates four simple current mirrors (Q3, Q14 and Q6, Q15 and Q7, Q16 and Q11, Q17). The bias current I_1 is generated by a Proportional To Absolute Temperature (PTAT) current generator. The resistor R_{1A}, serving as local feedback, can generally be neglected in the context of controlling the open-loop gain of the OA.

This structure provides a substantial current for charging the capacitor. Taking transistor Q4 as an example, when a large positive step signal is applied, I_{MAX} can in-

crease continuously until the gate voltage of Q4 reaches $V_{DD}-V_{Th3}$.

$$I_{MAX}=I_{D4}(V_{G4MAX})=\frac{K_4}{2}((V_{DD}-V_{Th3})-V_{Th2})^2 \quad (6)$$

This current is typically in the mA, which is significantly higher compared to the usual μA. Furthermore, from the circuit structure, we can observe that the slew rate of the OA primarily depends on the maximum current used to charge the capacitor, i.e.,

$$SR=\frac{I_{MAX}}{C} \quad (7)$$

When the value of C is fixed, the required slew rate can only be achieved by adjusting the value of I_{MAX}.

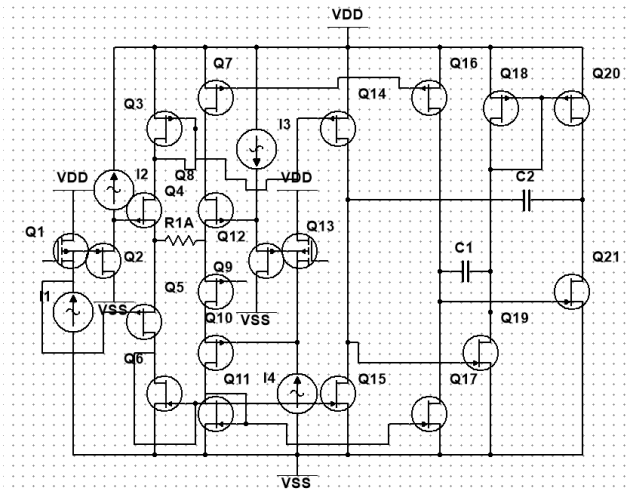

Fig. 5 Main Schematic of OA

3. Summary

This paper aims to discuss methods to enhance the operating speed of low-power OAs. It introduces three approaches: FDA, 2-stage OTA, and a novel "diamond transistor" high-speed OA. The FDA is proposed from a manufacturing perspective. As fabrication technology advances, we can continuously reduce channel length, thereby increasing operational speed. However, this might lead to performance degradation, hence the introduction of fully differential amplifier technology. This technology maintains the performance of the OA without excessively increasing power consumption, while meeting the requirements for higher speeds.

The 2-stage OTA is the result of improvements made by comparing Differential Amplifier and Telescopic Amplifier. The initially proposed Differential Amplifier is a basic amplifier with several limitations, such as design structure and restricted output swing. Consequently, it was improved to a Telescopic Amplifier, primarily aiming to enhance gain and bandwidth while maintaining low power consumption. By introducing a cascode configuration, the Miller effect is significantly reduced, improving frequency response. The final evolution into a 2-stage OTA was driven by the need for further increased gain and output swing, achieved by adding a second gain stage. This two-stage design provides higher gain and larger output swing but requires more complex frequency compensation to ensure circuit stability.

The novel "diamond transistor" high-speed OA represents an improvement from the perspective of the transistor itself rather than the circuit structure. By altering certain aspects of the transistor structure and adjusting the current source, speed enhancement is achieved.

Recently, high-speed low-power OA circuits have become a research focus, with ongoing optimization of circuit designs and upgrades to internal transistor structures. If transistor dimensions can be further reduced, the resulting speed improvements will be even more significant. This paper acknowledges some limitations, as circuit structures can be further optimized and gate-level implementations are not considered, potentially making them less suitable for large-scale circuits. These aspects represent areas for future improvement.

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