ISSN 2959-6157

Developments and Applications of Field-Effect Transistor

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Abstract:

This review article delves into the development and future prospects of Field-Effect Transistors (FETs), tracing their evolution from the nascent theoretical concept proposed by Julius Lilienfeld in 1925. Over the years, FETs have traversed significant milestones, marking their progression from fundamental ideas to practical applications. Key among these milestones are the advent of the Metal-Oxide-Semiconductor FET (MOSFET), which revolutionized the electronics industry, the Fin FET, offering enhanced performance through three-dimensional structures, and the Gate-All-Around FET (GAA-FET), promising even greater control and efficiency. It provides a systematic comparison of these technologies, dissecting their structural differences, evaluating performance metrics such as speed, power consumption, and scalability, and exploring their potential applications across diverse domains. While recent advancements in FET technology have primarily focused on structural innovations to mitigate the short channel effect, researchers are also actively exploring alternative avenues, including the use of novel materials and refined fabrication techniques, to further enhance FET performance and unlock new possibilities for electronic devices. This multifaceted approach underscores the dynamic and ever-evolving nature of FET technology, positioning it as a cornerstone for future advancements in electronics.

Keywords: Mos-FETs, Fin-FETs, GAA-FETs

1. Introduction

Semiconductors are a very important part of the electronics industry. And one of the important components is MOS-FET. In order to make fet smaller, more accurate, faster, energy-efficient, and easier to produce, major companies are constantly updating the materials and structures of fet. The FET has experience the development from Mos FET to the GAA FET which is currently being researched by several major internet companies. The overall improvement idea is to make the FET from a flat surface into a three-dimensional structure and then stack it up. The change of structure effectively reduces the limitation of short channel effects on FET size. And now, among the latest technologies, there are Ribbon Field Effect Transistor(Ribbon FET) from INTEL, vertical-transport nanosheetfield-effect transistors(VT-FET) from SAMSUNG and IBM as well as the Complementary FET(CFET) from IMEC.All of these are still in the research stage at present and have not yet been mass-produced.

This review will introduce the development history,future development and the problems faced by the whole industry.

2. Litmit of MOS-FETs and FIN-FETs

2.1 The origin of MOS-FETs

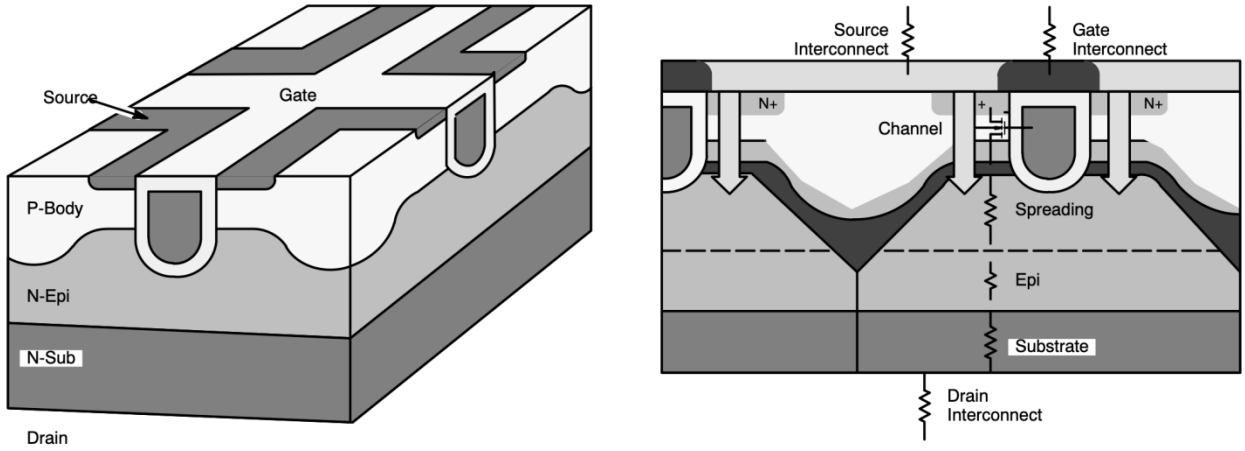

Fig. 1 Trench DMOS 3D cross-section, with associated resistive elements [1].

The development of FETs can be traced back to the invention of the point-contact transistor by William Shockley, John Bardeen, and Walter Brattain in 1947. However, the MOSFET, which revolutionized the semiconductor industry, was a later invention. The point-contact transistor used two closely spaced gold contacts on a germanium crystal. This design, while groundbreaking, was soon superseded by more stable and reliable transistor structures. However, the efficiency of this structure is too low, so scientists have developed MOSFET As shown in Fig.1.

In 1962, F.P. Heiman and S.R. Hofstein made significant modifications to the existing IGFET (Insulated Gate Field-Effect Transistor) structure, marking an important milestone in the field [2]. Building upon this foundation, the duo, now joined by Steven Hofstein (assuming a possible typographical error in the previous mention, as Frederic is likely a misspelling of F.P.) and Frederic (corrected) Heiman, published their seminal work on silicon MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) in 1963 [3]. This groundbreaking research earned widespread recognition and accolades from the semiconductor industry, further solidifying their contributions to the advancement of semiconductor technology.

2.1.1 The limit of MOS-FETs

As MOSFET continue to decrease to improve the performance and efficiency of chips while reducing power consumption and costs, the problem of short channel effects has emerged. The short-channel effects arise from two distinct physical phenomena that fundamentally alter the behavior of transistors. Firstly, there is a constraint on the electron drift properties within the channel, which restricts their movement in shorter channel geometries. Secondly, the reduction in channel length leads to a modification of the threshold voltage, a critical parameter determining transistor operation. In summary, these two factors – the limitation on electron mobility and the alteration of threshold voltage – collectively contribute to the short-channel effects observed in modern transistors [4].

“The short-channel effects in modern transistors are interconnected and synergistically impact device performance and reliability. These effects can be categorized into five main phenomena: Firstly, drain-induced barrier lowering and punchthroughemerge due to the heightened electric field proximal to the drain. This intensification results in a diminished barrier that confines electrons within the channel, potentially escalating to punchthrough, where the depletion region expands uncontrollably. Secondly, as the channel length decreases, surface scattering becomes more prevalent. The increased frequency of electron-surface interactions is like cars (electrons) navigating a bumpy road (channel surface), slowing down their overall speed (mobility) and thus reducing the device’s performance. Furthermore, velocity saturation manifests when electrons in the channel, subjected to high electric fields, approach their maximum drift velocity. This phenomenon restricts further current escalation despite an increase in the applied voltage, thereby limiting the device’s operating range. Additionally, impact ionization occurs under intense electric fields, where high-energy electrons knock other electrons out of their atomic bonds, creating a cascade effect. This is like a chain reaction in a nuclear reactor, leading to device degradation and increased leakage currents, much like radiation leakage in a poorly controlled reactor. Lastly, under strong electric fields, some electrons gain exceptionally high energy, becoming ‘hot.’ These hot electrons,

like overheated particles, can damage the device structure, particularly by penetrating the gate oxide. This is analogous to how overheated steam can damage the pipes in a boiler system, compromising the overall reliability of the device. In conclusion, the short-channel effects of drain-induced barrier lowering and punchthrough, surface scattering, velocity saturation, impact ionization, and hot electrons, collectively and synergistically, pose significant challenges to the performance and reliability of modern transistors with shortened channel lengths [4].

2.1.2 The discovery of FIN-FETs

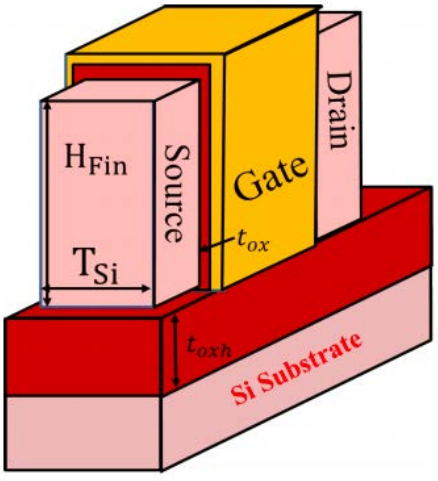

Fig. 2 Schematic diagram of conventional FinFET [5].

In 1999, Dr. Chenming Hu, a renowned electrical engineer and professor specializing in semiconductor devices and technology, made a groundbreaking discovery: FinFET technology as shown in Fig.2. This innovation aimed to minimize the detrimental effects of short-channel phenomena on Field-Effect Transistors (FETs) to the greatest extent possible. By introducing the FinFET design, Dr. Hu revolutionized the field, offering a solution that significantly reduced the impact of these effects and paved the way for more efficient and high-performance transistor operation. The introduction of triple gate-based Fin-shaped Field-Effect Transistors (FinFETs) has revolutionized transistor design by significantly enhancing gate controllability over the channel and optimizing leakage issues. Compared to traditional planar transistor architectures, FinFETs boast remarkable improvements in both performance and power efficiency. Their unique Fin-like structure facilitates superior control over current flow, effectively minimizing leakage and accelerating switching speeds. Over the past decade, FinFET technology has gained widespread adoption across diverse fields, particularly in the realm of mobile devices, where its advantages are most pronounced. In summary, FinFETs have emerged as a game-changer in transistor technology, driving advancements in performance, efficiency, and application versatility [5] .

2.2 The limit of FIN-FETs

While FinFET technology has significantly enhanced the performance of integrated circuits, it also exhibits several crucial limitations as the dimensions continue to shrink. Firstly, the short-channel effects intensify, leading to increased leakage current and static power dissipation, posing a bottleneck for further performance optimization. Secondly, the instability of the threshold voltage becomes more pronounced due to quantum effects, impacting the switching characteristics of the transistor. Furthermore, the complexity and cost of the manufacturing process escalate significantly with heightened process requirements, presenting challenges for production. Additionally, the amplification of corner effects may result in uneven device performance and reliability issues, while the slowdown in SRAM scaling threatens to halt the continuation of Moore's Law. To address these challenges, the industry is actively exploring new transistor architectures and manufacturing technologies, such as Gate-All-Around (GAA) transistors, aiming to overcome the limitations of FinFETs while maintaining performance gains.

3. GAA-FETs

3.1 GAAFET: Revolutionizing Transistor Scaling Beyond 5nm

GAAFET is an Emerging Candidate for Future Transistor Scaling. In the relentless pursuit of Moore's Law, researchers have turned to Gate-All-Around Field-Effect Transistors (GAAFETs) as a revolutionary solution to surpass FinFETs for sub-5nm technologies, offering unprecedented control over transistor channels. As the semiconductor industry progresses towards the 3-nm and even smaller nodes, the challenges posed by short channel effects (SCEs) such as subthreshold slope (SS) degradation and drain-induced barrier lowering (DIBL) have become increasingly significant. GAAFETs, with their gate structure wrapping around the channel from all sides, offer improved electrostatic control over the channel, making them a viable option to address these scaling issues.

GAAFETs come in two flavors: lateral nanowires (LNWs), resembling ultra-thin cylinders, and lateral nanosheets (LNSs), more like flattened ribbons. Each design offers unique advantages in the nanoscale realm. LNWs, with their cylindrical shape, offer superb gate control - imagine a water pipe completely surrounded by a control valve. However, this design comes at a cost: a smaller 'pipe'

means less water flow, or in transistor terms, reduced drive current. LNSs attempt to solve this dilemma by offering a wider channel - think of a flattened pipe allowing more flow. The performances of FinFETs, GAA-LNWs, and GAA-LNSs are comprehensively analyzed using an advanced device simulator, TCAD Sentaurus. The focus is on understanding the electrostatics and effective drive current (Ieff) in these architectures as they are scaled down to dimensions relevant for the 3-nm node and beyond.

The results indicate that while GAA-LNWs exhibit improved SS and DIBL compared to FinFETs, their reduced channel area limits their current driving capability. On the other hand, GAA-LNSs, with their larger channel area, offer better current driving capabilities but suffer from electrostatic control issues at smaller gate lengths. As a result, a careful trade-off between channel area and gate control is necessary when designing GAAFETs for future technologies.

Furthermore, the study explores the use of SiGe channels in p-type GAA-FETs, which enhances carrier mobility but also leads to a loss in subthreshold control. Overall, the research highlights the potential of GAAFETs in enabling further transistor scaling, but also underscores the need for innovative solutions to address the emerging challenges.

In conclusion, GAAFETs represent an exciting new frontier in transistor design, offering a path forward for the semiconductor industry as it navigates the challenges of scaling beyond the 5-nm node. With continued research and development, GAAFETs hold the promise of delivering faster, more efficient transistors for future electronic devices.

3.2 The development of GAA-FETs

The key dimensions projected for transistor scaling, as referenced in Table 1, are based on a scaling factor of approximately 0.7 times reduction in each generation, with specifications derived from recent advancements and expectations for future technologies [6][7]. These specifications highlight the challenges faced in transistor scaling, particularly at the 5-nm node and beyond, where increased short channel effects (SCEs) become a major concern as gate length (Lg) is reduced to accommodate spacer and source/drain (S/D) contacts.

In this context, the transition from a 5-nm thin and 43-nm-tall fin to a four-stacked gate-all-around lateral nanowire (GAA-LNW) structure was motivated by the need for stronger gate control. However, this transition led to a 63% loss in active channel area, resulting in significant loss of effective drive current (Ieff) and increased parasitic capacitances [8][9].

To mitigate these issues, the GAA-LNW was further modified into a gate-all-around lateral nanosheet (GAA-LNS) , which increased the channel area compared to the GAA-LNW. Nevertheless, even with the GAA-LNS, scaling down the contacted gate pitch (CGP) to 24 nm is projected to result in significant electrostatic and Ieff losses, as well as increased parasitic effects, for a targeted OFF-state current.

In addition to LNWs and LNSs, researchers are exploring the ‘U-shaped FET’ (UFET) architecture. This innovative design, resembling a U-shaped channel, offers another approach to tackle the challenges of scaling towards and beyond the 3-nm node. The specifications and comparisons mentioned are aligned with the projected key dimensions outlined in Table 1.

Table 1. Projected Scaling Dimentions For 5-nm Node and beyond [10]

Technology node	N5	N3	N1
Contacted Gate Pitch (CGP) (nm)	32	24	14
Metal Pitch (MP) (nm)	24	18	14
Gate Length (Lg) (nm)	14	10	8
Effective Oxide Thickness (EOT) (nm)	0.57	0.57	0.57

4. Conclusion

The journey of Field-Effect Transistors (FETs) from Mos-FETs to Fin-FETs and now Gate-All-Around (GAA) FETs is like watching a caterpillar transform into a butterfly - each stage representing a leap in innovation and performance in the semiconductor industry. The driving force behind this evolution is the semiconductor industry’s constant battle against short-channel effects - the microscopic gremlins that emerge as transistors was shrinked to near-atomic scales. Mos-FETs, the pioneering yet inefficient ancestors, gave way to MOSFETs and later FinFETs - each generation like a new breed of watchdog, offering tighter control over the electronic ‘fence’ (the gate) and reducing unwanted ‘escapes’ (leakage). Despite their improvements, FinFETs still struggle with electronic ‘leaks’,

unpredictable ‘on-off switches’ (unstable threshold voltages), and intricate ‘assembly lines’ (complex manufacturing). These challenges have pushed researchers to explore the next frontier: GAA transistors.

GAA MBCFETs represent a paradigm shift - imagine a gate that completely envelops the channel, like a glove fitting perfectly around a hand. This 360-degree control promises to tighten the electronic ‘leash’, minimize ‘energy waste’, and boost overall performance beyond what FinFETs can achieve.Their fabrication, though complex, is being refined for cost-effectiveness. Industry leaders like Samsung, TSMC, and Intel are transitioning to GAA MBCFETs for advanced scaling. Alternative channel materials like germanium, III-V compounds, and 2D materials are being explored to transcend silicon’s limitations.

Novel device architectures, including TFETs, CNTFETs, and NCFETs, cater to specialized applications. To realize these innovations, the industry invests in advancing manufacturing techniques and leveraging AI for optimization. Addressing quantum effects, manufacturing variations, and reliability becomes crucial as devices shrink.

This holistic approach, combining innovative device designs, alternative materials, advanced manufacturing, and intelligent optimization, enables the semiconductor industry to surmount scaling barriers and meet the evolving demands of the global electronics market, shaping its future trajectory in consumer electronics, high-performance computing, and IoT.

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