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Research on Chip Manufacturing and Fault Detection Technology

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Abstract:

In the wave of the digital era, the chip plays a key role in promoting the whole information technology revolution with its core position in the development of world science and technology. As the cornerstone of computing and data processing, the development of chips has promoted the progress of the entire technology field. The chip's manufacturing is the key to determining the performance and computing power of the whole chip, and fault detection technology in the production process is an important part of determining the product's quality and cost. Therefore, under the background of Moore's law approaching the physical limit, how to ensure the yield of chip production while continuing to improve chip performance has become a major challenge for the chip manufacturing industry. Based on this, this paper summarizes the key manufacturing steps of the chip. The chip manufacturing technology is comprehensively sorted from design to silicon wafer manufacturing, photolithography, etching, ion implantation, and other processes. At the same time, the research direction of monocrystalline silicon manufacturing technology and the existing lithography technology are introduced, including optical lithography, extreme ultraviolet lithography, electron beam lithography, and so on. Fault detection technology in chip production has also been introduced. In addition, the chip manufacturing and fault detection technology introduced in this paper is summarized and its future development is prospected, which provides reference and inspiration for promoting the continuous progress of chip technology.

Keywords: Chip Manufacturing; Monocrystalline Silicon; Lithography Technology; Fault Detection

1. Introduction

In today's digital age, the chip is the core of information technology. It plays an indispensable role in various industries and fields and promotes the progress of the whole society. However, the technical development of the chip is extremely difficult and has now reached the bottleneck stage. Chip manufacturing is the core aspect of the semiconductor process, and it is the key node that affects whether the computing power of the semiconductor chip can be given [1]. The precision of its manufacturing process is directly related to the performance, stability and yield of electronic products. With the rapid development of semiconductor technology, the chip manufacturing process has entered the 3-nanometer or even 2-nanometer scale. Any small defect may lead to the failure of the whole chip function. Therefore, in semiconductor manufacturing, defective wafer detection and related chip fault detection techniques are crucial to prevent yield losses due to process abnormalities [2].

This paper will first introduce the key steps of chip manufacturing, from design, silicon wafer manufacturing, photolithography, etching, ion implantation, annealing, film deposition, and chemical mechanical polishing to the interconnection process. Subsequently, this paper will introduce the current research on monocrystalline silicon manufacturing, and analyze the advantages and disadvantages of several existing lithography technologies. Provide readers with a comprehensive understanding of the current semiconductor manufacturing technology. At the same time, this paper will also introduce the new technology of fault detection in chip production, including the Bayesian network-based semiconductor production fault detection method and wafer surface defect detection based on machine learning. These technologies can effectively improve the efficiency of chip fault detection, and give a new idea of technology development.

The first chapter of the paper is the introduction. Firstly, it introduces the research background and significance of the paper, as well as the general introduction of the content of this paper. Chapter 2 is an overview of the chip manufacturing process, and gives the general process flow of the chip manufacturing. Chapter 3 is about the existing chip manufacturing technology. Introducing the research direction of monocrystalline silicon manufacturing technology, and analyzing the advantages and disadvantages of the existing modern lithography technology. The fault detection methods and techniques in chip production are given

in Chapter 4. Finally, the conclusion part summarizes the full text and prospects for future chip technology. The last part is the conclusion, which summarizes the full text and prospects for future chip technology.

2. Overview of Chip Manufacturing Process

Chip manufacturing is divided into two parts: design and manufacture. In the design phase, the hardware description language (HDL) is used to describe the structure and behavior of the digital system hardware in text form, and the function of the chip is written in code to form a complete HDL code. Then HDL code is converted into a logic circuit diagram and physical circuit diagram by EDA software. Next is the silicon wafer manufacturing stage. This process starts from the deoxidation and purification of quartz ore. After obtaining pure SiO2, carbon is added for high-temperature refining, and high-purity silicon crystals are gradually extracted and acid-washed to remove impurities to obtain high-purity polysilicon. After that, polycrystalline silicon was made into monocrystalline silicon rods by the Czochralski (CZ) method. After a series of processes such as rolling, cutting, chamfering, polishing, cleaning and oxidation coating, the required silicon wafers are finally obtained. Then the most critical and difficult lithography process. In this step, the chip design pattern is transferred to the silicon chip, and the circuit diagram is engraved in the lithography machine through the ultraviolet light through the mask irradiation and exposure of the photoresist. Rinse the unexposed photoresist and apply the developer solution. The fins in the fin field effect transistor are formed by etching techniques such as plasma physical impact. Finally, the covered photoresist and impurities are cleaned. The next step is ion implantation. In the ion implantation machine, high-speed and high-energy ion beams are injected into the silicon wafer to change its carrier concentration and conductive type to form different device structures. Rapid thermal annealing (RTA) is usually performed after ion implantation to eliminate lattice damage and activate doped ions. Then, thin film deposition was carried out using physical vapor deposition (PVD), chemical vapor deposition (CVD), or atomic layer deposition (ALD) techniques to form different material layers on the silicon wafer. Then it was polished by chemical mechanical polishing (CMP). Finally, through the interconnection process, different transistors and electronic components are connected by conductive materials such as copper to form a complete circuit. The above chip manufacturing process steps are shown in Fig.1.

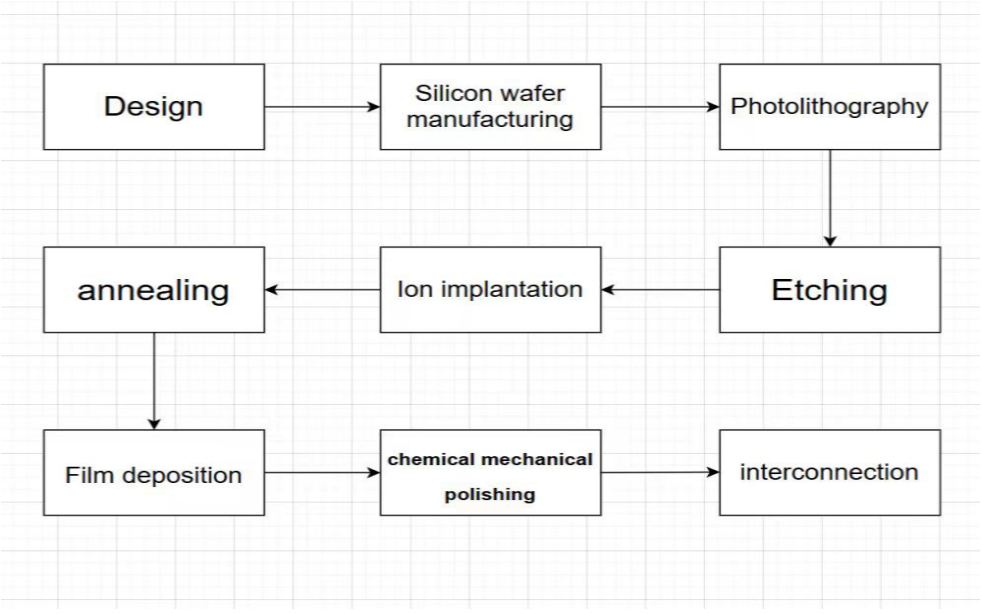

Fig. 1 Chip manufacturing process steps

The entire manufacturing process may need to repeat the above process dozens of hundreds of times, and through multilayer routing, packaging and testing steps, to finally get the required chip products.

3. Current Chip Manufacturing Technology

3.1 Monocrystalline silicon manufacturing technology

Generally, the preparation methods of monocrystalline

silicon are the CZ method and zone melting method. Up to now, most of the monocrystalline production uses the Czochralski method. Czochralski monocrystalline silicon currently accounts for the highest proportion in the crystal silicon market, reaching more than 90 % [3]. At present, the manufacturing technology of monocrystalline silicon has become mature, and the mode is relatively fixed. Researchers are more inclined to study the crystal defects (including point defects, line defects, face defects and bulk defects) in Czochralski silicon. Defects in silicon will lead to a decrease in the yield of gate oxide integrity, insulation failure, capacitance short circuit and junction leakage [4]. Concurrently, nitrogen, phosphorus, boron, carbon and other impurity atoms and oxygen will cause related defects [5]. Solving the problem of crystal defects has become the key to improving the manufacturing technology of monocrystalline silicon.

3.2 Modern Lithography Technology

In recent years, various advanced lithography technologies have been introduced, including optical lithography, extreme ultraviolet lithography (EUV), electron beam lithography (EBL) [6], X-ray lithography and ion beam lithography [7]. Selecting the optimal lithography technology is contingent upon the integrated circuit production costs in addition to factors such as performance, resolution, and registration accuracy. The advantages and disadvantages of the above six lithography techniques are shown in detail in Table 1.

Table 1. Comparative analysis of the advantages and disadvantages of lithography technology [8-12]

Lithography Technology	Advantages	Disadvantages
Optical lithography	Chips can be produced in vast quantities at once. Time-saving and fast; Low manufacturing costs	Limitations that do not apply to curved surfaces; Sometimes there is a mismatch between the light source and the photoresist
EUV lithography	High resolution and throughput; Existing an EUV lithography method with no etching resist, and further development can overcome the inherent resolution and roughness limitations of photoresist materials	High cost and great difficulty; The EUV light source has a short wavelength and needs to operate in a vacuum environment; High equipment maintenance and operation costs
EBL	The electron wavelength is small and has the highest actual resolution	Due to the serial nature of the operations, the throughput is quite low; There are limitations to the photoresist's sensitivity and the electron beam's intensity
X-ray lithography	Low price; High throughput; The wavelength of X-ray is shorter than the ultraviolet used in lithography, so it has a higher resolution and no diffraction limit	The alignment of the masks can be disturbed by vibrations, and if the masks are not correctly positioned on the wafers, the transistors on the wafer will not function as intended; EBL is the method used to create X-ray masks, and it is a very slow procedure
Ion beam lithography	Superior for creating 3D constructions with a high aspect ratio; By altering the ion energy, the ion beam's penetration depth can be precisely determined	Requires a high vacuum environment and is time-consuming; Ion beams can upset the wafer structure, leading to doping or other consequences; Complex patterning using stencil mask technology raises the cost of mask manufacture per level and necessitates the usage of a complimentary mask

Dual-beam super-resolution lithography	By suppressing the photopolymerization brought on by the writing light at the hollow ring, the suppression beam of the hollow circular form is employed in the dual-beam lithography technique to improve resolution and reduce feature size; It is an improvement of traditional UV lithography technology; The equipment on the manufacturing line can be improved and replaced at a reduced cost without sacrificing the current industrial lithography experience	When the lithography equipment is affected by the external environment, such as vibration, temperature change and other factors, the relative position of the lithography equipment may shift to a certain extent, resulting in the separation of two beams of light; Certain particular cases are still being researched, and the technology is not developed enough.

Each lithography technology has its specific application scenarios and advantages. However, for now, EUV lithography technology has become the mainstream choice of current technology nodes because it can achieve smaller feature sizes. However, EUV lithography technology also has many problems, such as huge energy consumption, low energy utilization, complex design and manufacture of optical systems, and reaching the limit of Moore's law. Therefore, the application of other lithography technologies and the research of new lithography technologies are very essential.

The remaining processes in the chip manufacturing process are relatively fixed compared with monocrystalline silicon manufacturing technology and lithography technology. Therefore, this paper only focuses on the above two technologies, and the remaining processes are no longer described.

4. Fault Detection in the Chip Production Process

In addition to the current common and common detection methods, such as physical detection method (including X-ray detection, ultrasonic detection, etc.), electrical detection method (including static parameter test, dynamic parameter test, etc.) and logic detection method (including logic analyzer test, boundary scan test, etc.), this paper will introduce two new detection methods.

4.1 Bayesian Network-based Semiconductor Production Fault Detection Method

A Bayesian network-based half-body manufacturing defect prediction method is developed in [13]. The construction and prediction technique of the Bayesian network is provided, and the fault conditions of each production step and the state parameters in the production process are taken as variables. And contrasted with other methods like decision trees, support vector machines, artificial neural networks, and so on. Ultimately, an effective chip fault detection method is achieved.

4.2 Wafer Surface Defect Detection Based on Machine Learning

The main goal of machine learning is to utilize mathematics to solve both the model and the problem by first turning a given problem into a mathematical model. After that, assess how the model affects this issue. It is separated into three categories: semi-supervised learning, unsupervised learning, and supervised learning based on the features of the training data [14]. Supervised learning is a learning model [15], constructed from labeled training data, and the necessary new data samples are predicted using this model. Additionally, it is a machine learning technique that is widely used in the identification of wafer surface defects and has outstanding robustness in the target detection area. The unsupervised clustering approach is frequently used to identify complicated wafer defect patterns because of its excellent tolerance to irregular features of defect patterns on wafer patterns and unequal classification. A machine learning technique called semi-supervised learning blends supervised and unsupervised learning [16]. A significant amount of unlabeled data and a small amount of labeled data can be used to solve the problem when semi-supervised learning is applied.

It can be seen from the above that the Bayesian network-based semiconductor production fault detection method is based on the mathematical model, relying on the model structure and the parameters in the production process to predict and detect the fault. It has made an effective supplement in the rare prediction of faults. The wafer surface defect detection based on machine learning can adapt to different types of wafer surface defect detection. And its three learning methods can complement each other, effectively reducing the impact of classification and cost consumption.

5. Summary

This paper first outlines the key process of chip manufacturing, and then introduces the research direction of monocrystalline silicon manufacturing will be based on crystal defects. The analysis is done on the advantages and disadvantages of the six lithography methods now in use, which are optical lithography, EUV lithography, EBL, X-ray lithography, ion beam lithography, and dual-beam super-resolution lithography. Simultaneously, two novel methods for fault detection in chip manufacturing are presented: the Bayesian network-based semiconductor production fault detection method and wafer surface defect detection based on machine learning. Of course, space constraints prevent this study from covering every relevant technology linked to fault detection and new chip manufacture. Readers must continue to do further research after being inspired by this paper to achieve a deeper understanding.

Chip manufacturing and fault detection technology are the cornerstones of information technology progress, and it is developing towards diversification, intelligence and innovation. It is hoped that readers can understand the existing chip manufacturing and fault detection technology from this paper, find the development direction of chip manufacturing, and put forward new technical methods to advance the fault detection technology. While helping to break through the bottleneck of high-precision chip manufacturing as soon as possible, improve the yield of chip production, and realize the double progress of technological breakthrough and cost reduction. Discover a new way out in the challenge of Moore's law approaching the physical limit, and make outstanding contributions to global scientific and technological progress.

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