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Research on Low-Power Digital Integrated Circuit Technology

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Abstract:

In today's diverse and rapidly developing field of low-power technologies, various industries are actively applying these advanced technologies to practical production in order to reduce energy consumption and mitigate environmental pollution. Based on this core concept, this article delves into and compares the principles, advantages, and disadvantages of the low-power technology of passive tag chips with the representative low-power technologies of dual-power and crossed-zero clocking, as well as their respective application areas. Specifically, the article conducts a detailed comparative analysis of the low-power technology of passive tag chips versus dual-power and crossed-zero clocking technologies from three perspectives: power consumption, design approach, and practical application. Through in-depth research, it was found that the low-power technology of passive tag chips holds significant advantages in the logistics industry, making it particularly well-suited for this field; meanwhile, dual-power and crossed-zero clocking technologies perform better in high-performance computing, making them more appropriate for such an application environment.

Keywords: Low-power consumption, Passive tag chip, Dual-powe, crossed-zero clocking technology

1. Introduction

In today's rapidly developing era, the focus of research has gradually shifted from solely pursuing speed to reducing energy consumption. With the rapid advancement of technology, we are inevitably facing some undesirable side effects, such as environmental pollution and excessive energy consumption. Therefore, it is imperative to take effective measures to mitigate these negative impacts, which has led to the rise of research on low-power technologies. It is undeniable that various low-power technologies have emerged in society today. These technologies are widely applied across different fields, from electronic devices to industrial production, all embodying the pursuit of minimizing energy consumption [1].

Additionally, low-power technologies play an important role in architectural design and urban planning. By adopting efficient insulation materials and smart lighting systems, the energy consumption of buildings is effectively controlled [2]. The integration of electric vehicles and smart grids is also progressing, including the charging and discharging characteristics of electric vehicles and their interaction with the grid. Through an orderly charging and discharging control strategy, the impact of electric vehicles on the grid after being connected can be reduced, and the flexibility of grid operation can be improved [3]. In the field of the Internet of Things, low-power technologies such as LPWAN, Bluetooth 5.0, Zigbee, and LoRa are being widely used. These technologies allow devices to achieve long-distance data communication with extremely low energy consumption, thereby extending the lifespan of devices and reducing maintenance costs [4]. In architectural design and urban planning, low-power technologies also play an important role. For example, by using efficient insulation materials and smart lighting systems, the energy consumption of buildings is effectively controlled [5]. In summary, low-power technology has become an inevitable trend in today's social development. Through continuous research and innovation, we expect to achieve more efficient and environmentally friendly energy utilization in various fields in the future, contributing to sustainable development [6].

The content of this article is based on the theory mentioned above and provides a comparison of two different low-power technologies. One is the low-power technology for UHF RFID passive tag chips based on the ISO18000-6C standard [7], and the other is the dual power supply and cross-zero clock technology that leads to low noise and high efficiency in digital integrated circuits [8]. This article elaborates on the advantages and disadvantages of the different low-power technologies, identifies their applicable fields, and offers prospects for the future development of both technologies.

Chapter 1 serves as the introduction, first presenting the background and significance of the research. Chapter 2 focuses on technical analysis and comparison, explaining

the principles of both technologies in detail and conducting an in-depth comparison. Finally, in the conclusion section, the article summarizes the research and provides an outlook on future development.

2. Definition and Principles of the Technology.

2.1 Low-Power Technology for UHF RFID Passive Tag Chips Based on the ISO18000-6C Standard.

Radio Frequency Identification (RFID) technology is an advanced automatic identification technology [9]. With its advantages of being contactless, having flexible reading and writing capabilities, fast processing, long-distance recognition, and high security, it is widely used in various fields such as logistics management, merchandise sales management, product manufacturing, and public information services. The foundation of its application is CMOS digital circuits [6], and the low-power performance is mainly reflected in the design of the low-power digital baseband circuit of ultra-high frequency passive electronic tags that comply with the ISO18000-6C standard.

CMOS circuits are composed of NMOS and PMOS transistors in a complementary configuration. Their energy consumption includes both dynamic power consumption and static power consumption. $P_{dynamic}$, The dynamic power consumption is caused by the charging and discharging of parasitic capacitances in the circuit, while the static power consumption is generated by leakage currents.

$$P_{total} = P_{dynamic} + P_{leakage} \qquad (1)$$

Static power consumption, also known as leakage power consumption [10], includes components such as reverse-biased diode leakage current, gate-induced drain leakage current, subthreshold leakage current, and gate leakage current. On the other hand, dynamic power consumption occurs when the transistors switch states during chip operation, primarily consisting of dynamic switching power consumption (P_{sw}) caused by dynamic switching current and short-circuit power consumption (P_{sc}) generated by short-circuit current.

In studying this technology, the method used is power analysis through EDA tools [6]. EDA tools further divide the switching power consumption (Psw) within dynamic power consumption into two components: device power consumption and wire load power consumption. The applied power analysis model is shown in Fig.1.

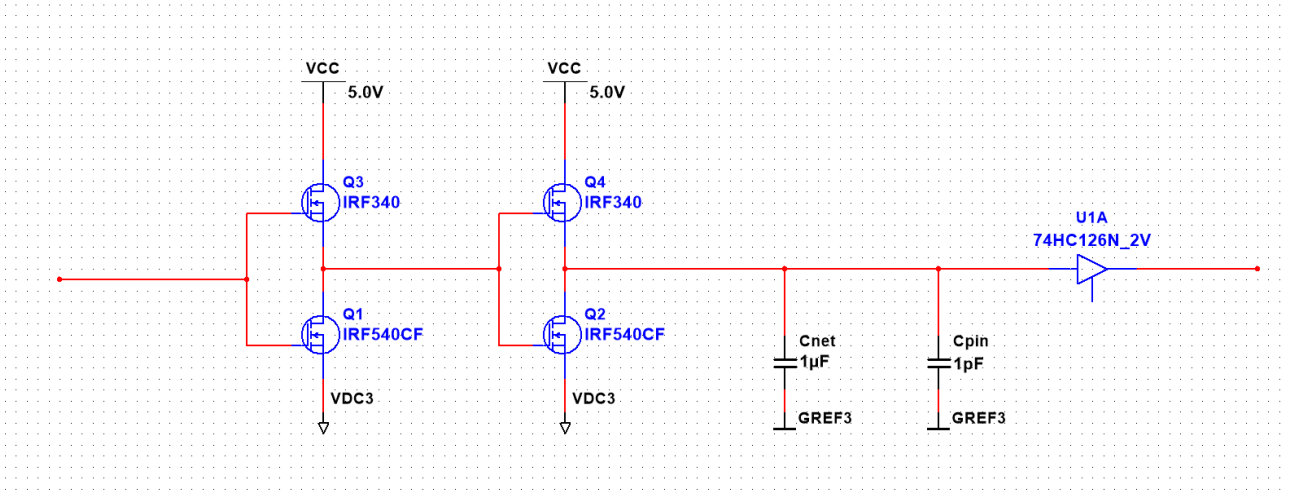

Fig.1 applied power analysis model

In the field of low-power design, this technology focuses on the low-power design of the digital front-end circuits for tag chips, covering several aspects, including system low-power design, decoder module design, encoder module design, cyclic redundancy check (CRC) and calculation module design, as well as state machine module design. This article focuses on system low-power design.

In system low-power design, the technology achieves modular division of the system. First, the decoder decodes and filters the received signals. The signals then flow into two paths: one path is directed to the input preprocessing module, which handles command parsing and preprocessing, while the other path goes to the CRC module, which performs cyclic redundancy checks. The state machine, as the control module, coordinates and manages the operation of all modules. It checks the CRC results and, based on the command parsing results, retrieves command data from the SPC module, analyzes the commands, and executes state transitions accordingly [7]. The state machine also operates the pseudo-random number generator, time

slot counter, and EEPROM memory, controlling the transmission of backscatter EPC+PC data and the contents of the EEPROM.

During data transmission, the state machine sets the backscatter mode and instructs the OCU to perform data preprocessing. It reads content from the EEPROM, writes it into the OCU module, and optionally calculates the CRC value, appending it to the data before sending it to the encoder. The encoder encodes the data into signals that comply with the frame format, which are then sent to the modulator for modulation and transmission. The state machine also controls the system clock module to generate the working clock required by each module. Additionally, the state machine, along with the pseudo-random number generator, time slot counter, and timeout counter, constitutes the anti-collision circuit, ensuring that collisions and conflicts are avoided during data transmission, thereby improving system stability and efficiency. The detailed flow is shown in Fig.2.

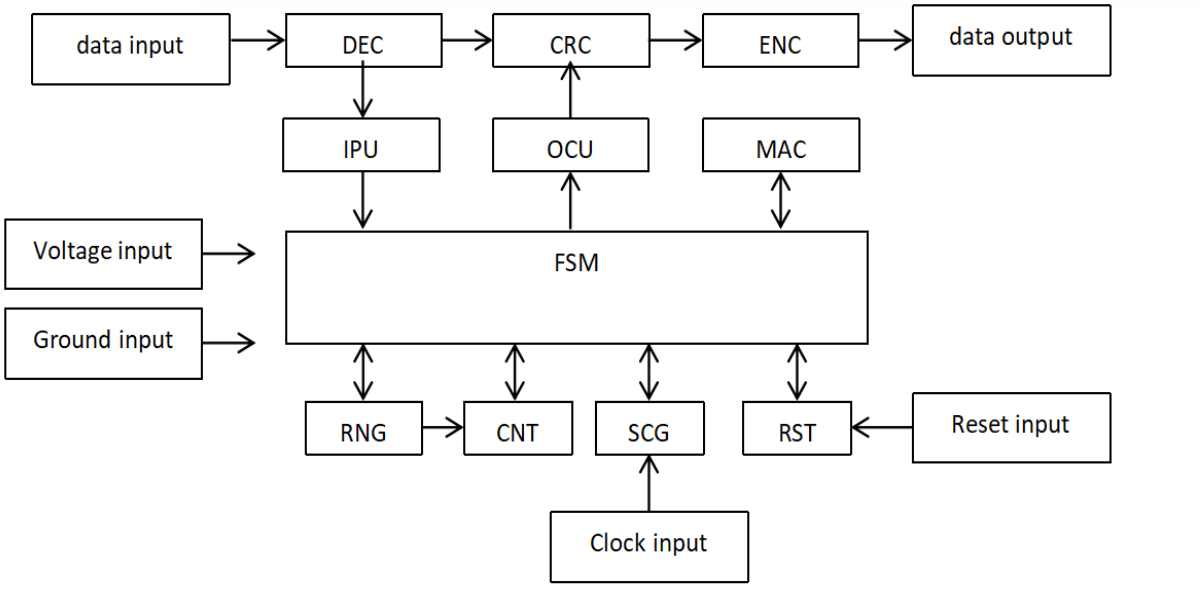

Fig.2 detailed flow

2.2 Dual Power Supply and Cross-Zero Clock Combination Technology.

This technology combines dual power supplies and cross-zero clocks to reduce power consumption and noise. The dual power supply refers to the application of both positive and negative power supplies, while the cross-zero clock means that the clock signal crosses zero between the positive and negative power supply voltages, rather than switching at a single voltage level. Cross-zero clocks can eliminate noise at certain frequencies, and the voltage level is grounded, ensuring reduced power consumption and improved energy efficiency.

The principles of this technology can be considered from five aspects: frequency domain analysis, three-level energy system, reduction of dynamic power consumption, consideration of static power consumption, and CMOS gate hysteresis curve.

In terms of the frequency domain, the clock voltage fluctuates between -V and V with a period of T. The clock phase can be marked as 0, P1, ..., Pi, Pi+1, ..., Pj, Pj+1, etc. Through Fourier transform, we can reveal the characteristics of the clock at phases P0 and P1. Fourier analysis of the clock signal shows that at certain frequencies, the signal is imaginary, meaning no noise is generated at those frequencies [11].

For the three-level energy system, electron-hole pairs become neutral at an intermediate energy level close to ground or at 0 volts, thus reducing power consumption.

As for dynamic power consumption, as mentioned earlier, it mainly arises from the charging and discharging of capacitors. By using dual power supplies and cross-zero clocks, the energy used for capacitor charging and discharging can be reduced without sacrificing performance, thus lowering power consumption. Regarding static power consumption, this technology points out that with dual power supplies, PMOS and NMOS transistors can be turned off by setting the input signal near zero voltage, reducing static power consumption.

Finally, concerning the hysteresis curve, it is noted that in a dual power supply system, there are two threshold voltages, which help maintain stable output voltage between states 0 and 1 [12].

3. Technology Comparison

In terms of power consumption, the first technology adopts a modular design and uses EDA tools to conduct power consumption analysis. In contrast, the second technology focuses on the frequency domain and energy system, comprehensively considering the characteristics of the clock signals and CMOS gates.

From a design perspective, the first technology primarily focuses on system-level design and the coordination between modules, while the second technology emphasizes power management and clock signal architecture.

In practical applications, the low-power digital integrated circuit technology for UHF RFID passive tag chips compliant with the ISO18000-6C standard is particularly well-suited for applications such as cargo tracking in logistics management, inventory control in merchandise sales management, and component identification in product manufacturing. Since low-power RFID tags can operate for long periods without the need for battery replacement, this significantly reduces maintenance costs. Therefore, in the real world, a large retailer might adopt this technology to track goods across its global supply chain, ensuring inventory accuracy and timely restocking. On the other hand, digital integrated circuits using dual power supply and cross-zero clock technology, characterized by low noise and high efficiency, are particularly suitable for high-performance computing equipment, such as servers and data centers, as well as embedded systems that require high reliability and low energy consumption. This technology allows servers to reduce energy consumption and heat generation while improving computing efficiency and stability. For instance, in data centers, it helps lower cooling costs and extend the lifespan of servers. Thus, in the real world, cloud service providers might deploy this technology in their data centers to optimize energy efficiency and reduce operating costs.

Overall, we can observe the application of both technologies in their respective fields and the practical benefits they bring. UHF RFID technology compliant with the ISO18000-6C standard mainly focuses on automatic identification and tracking functions, making it particularly suitable for environments that require precise identification and management of items. On the other hand, dual power supply and cross-zero clock technology is better suited for electronic systems that require high performance and reliability, especially in scenarios where there are strict standards for energy efficiency and system stability.

4. Summary

This paper finds that the focus has shifted from pursuing speed to reducing energy consumption in response to environmental pollution and excessive energy use. Low-power technology is widely applied in areas such as electronic devices, industrial production, architectural design, and urban planning, aiming to minimize energy consumption. As a result, its development is expected to become an inevitable trend in societal progress, promoting efficient and environmentally friendly energy use.

Next, the definition and principles of UHF RFID passive tag chip low-power technology can be summarized in four points: first, RFID technology is characterized by being contactless, having flexible reading and writing capabilities, fast processing, long-distance recognition, and high security; second, CMOS circuit energy consumption, which includes dynamic power consumption (switching power and short-circuit power) and static power consumption (leakage power); third, low-power design, analyzed through EDA tools, covering system low-power design, decoder modules, encoders, etc.; finally, system operation process, including signal decoding and filtering, preprocessing, CRC checks, state machine coordination, and data transmission. Many large retailers and logistics companies adopt this technology to improve efficiency and reduce power consumption.

As for the dual power supply and cross-zero clock technology, two key points can be summarized: first, its technical characteristics involve the application of dual power supplies, while cross-zero clocks reduce power consumption and noise; second, the principles of this technology include a wide range of considerations, such as frequency domain analysis, three-level energy systems, dynamic power reduction, static power consumption considerations, and CMOS gate hysteresis curves. This technology is commonly used in servers and data centers.

Finally, a summary of the technology comparison shows that UHF RFID technology employs a modular design and EDA tool analysis to evaluate power consumption, while dual power supply technology focuses on frequency domain and energy system considerations. From a design perspective, UHF RFID emphasizes system-level design, while dual power supply technology focuses on power management and clock signal architecture. In terms of applications, UHF RFID is suitable for logistics management and merchandise sales management, while dual power supply technology is more applicable to high-performance computing equipment and embedded systems.

This paper concludes that ultra-high frequency RFID technology (UHF RFID) primarily highlights its automatic identification and tracking functions. By utilizing radio frequency signals, this technology can quickly and accurately identify target objects and extract related information, making it widely used in industries such as logistics,

warehousing, and retail. On the other hand, dual power supply technology focuses on performance and reliability. Through dual power supply design, it ensures stable operation of devices in complex environments, thereby improving system reliability and safety.

Therefore, in future trends, low-power technology will achieve efficient and environmentally friendly energy use across more fields. By optimizing circuit design and improving power management, low-power technology can reduce energy consumption, extend device lifespans, and contribute to sustainable development. This will not only help reduce energy use and environmental pollution but also reduce business operating costs, offering dual benefits of economic and environmental advantages.

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