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Design and Implementation of a 7-Person Voting Device based on Quartus

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Abstract:

As the complexity of digital system design continues to increase, efficient and precise decision support systems have become increasingly important. This paper presents the design and implementation of a 7-voter decision system based on Altera's Quartus software. The voter is applied in the core decision-making process to ensure the accuracy and efficiency of decisions. The study begins by outlining the design principles of the 7-voter decision system, using a design philosophy that minimizes timing delays and optimizes hardware resource utilization. A complex majority voting logic circuit is implemented using high-level hardware description languages (VHDL/Verilog), ensuring the advanced nature and applicability of the voting circuit. In terms of the logical implementation of the voting circuit, the paper conducts an in-depth analysis of the optimization of combinational and sequential logic and standardizes the input and output to enhance the signal stability and the system's resistance to interference. On the Quartus platform, the design process of the voting system is elaborated in detail, with careful consideration given to boundary conditions and hardware compatibility. The implementation of the voter has undergone rigorous simulation and testing. Strict parameter setting for simulations and waveform analysis confirm the correctness of the circuit, and fault simulation tests further confirm its reliability. Performance indicators such as response time and percentage of resource utilization have been quantitatively analyzed and meet the design objectives set beforehand. Overall, this research not only realizes a high-performance 7-voter decision system but also provides an effective case study for applications on the high-performance Quartus design platform. Future research can build on the current work to further optimize algorithms and hardware, explore the potential for the application of the voter in a broader range of fields, and adapt to the new features of the Quartus platform to achieve more powerful decision support functions.

Keywords: Quartus Platform; 7-Person Voter; Digital System Design; VHDL/Verilog; Simulation Testing

1. Introduction

1.1 Research Background

In modern digital circuit design, as one of the important logic circuits, it is widely used in redundant system, fault detection and fault tolerance mechanism. In recent years, with the rapid development of FPGA and CPLD technology, the design methods based on hardware description languages (such as Verilog and VHDL) have gradually become the mainstream. The application of these technologies enables designers to implement complex logic functions flexibly and efficiently. In particular, Quartus II software, as an integrated development tool launched by Altera, is widely used for its strong FPGA development capabilities and good user interface.

Although there have been many research and applications of voting devices, there are still some challenges in the specific design and implementation of the seven-person voting instruments. Most of the existing studies focus on the basic principle and simple realization of the voting device, and the lack of in-depth discussion of its application in complex systems. In addition, how to effectively optimize circuit performance and resource utilization in practical design is still a big problem in current research. Therefore, the systematic design and implementation of the seven-person device based on Quartus can provide more reliable solutions for error detection and fault-tolerant systems.

This study will use the Verilog HDL language for the seven-person voting device design, simulation and verification by Quartus II software. First, the detailed design of the circuit logic will be carried out, followed by code writing and debugging, and finally, the correctness and performance of the design will be verified through experiments. At the same time, theoretical analysis and practical

operation will be combined in the research process to improve students' understanding and practical ability of digital circuit design[1].

1.2 Study content

This paper takes the design and implementation of the 7-person voting device based on Quartus as the research object, and discusses the basic principle of digital circuit design, aiming to realize an efficient and accurate voting system. With the continuous development of science and technology, electronic products are used in the network voting, election management and other fields more and more widely, especially in the case of multi-person voting, reliable electronic voting device is very necessary. Through the construction of the voting mechanism, this paper combines the characteristics of Quartus software, and shows the advanced nature and convenience of digital circuit design, so as to improve the efficiency and accuracy of the actual voting process.

This study focused on designing a voting instrument with seven voters and enabling it to implement multiple voting logic. In the design, we use the hardware description language (VHDL) for circuit programming, and make full use of the powerful functions of Quartus software, to achieve complex logical judgment. At the same time, through the design and implementation of the status machine of the voting results, to ensure that the voting machine can effectively process the voting records and output the final results. This study not only focuses on the function realization of the voting device, but also considers its stability and reliability in practical application to ensure the fairness of the voting process.

This research work mainly has the following parts: The first part, the introduction of Quartus software and its application, through the analysis of the software functions and usage scenarios. The second part details the design of the 7-person voting device, including requirements analysis, design ideas of hardware circuit, VHDL code writing and design verification. The third part focuses on the implementation and testing of the voting device to evaluate the performance and stability of the system. Finally, the summary and prospect, put forward suggestions for possible improvements in the future, and prospect the possible application of the technology in a wider range of fields.

The first chapter: the introduction mainly introduces the importance of the voting mechanism in the modern society, and expounds the necessity of designing the electronic voting device. In view of the defects of traditional voting methods, such as low efficiency and error-prone, this paper proposes the design and implementation of electronic voting device based on Quartus. At the same time, the introduction section briefly reviews the development process of related technologies, clarifying the background and significance of this paper[2].

The second chapter discusses the functions and application of Quartus software in detail, and analyzes its advantages in digital circuit design, especially in the aspects of design verification, simulation and integration. At the same time, combined with the case of software operation, it provides the detailed steps for digital circuit design with Quartus, striving to provide direct help to the researchers who need to use the software for design in the future[3].

Chapter 3 focuses on the design of a seven-person voting device. Through the analysis of the system requirements, the input force and output logic of the voting device are determined to ensure that the system can accurately identify and count the effective voting among the 7 voters. In addition, a finite state machine (FSM) is used in the design to control the voting process, so that different voting states can be effectively switched and make real-time response to the input. The design of each state and its conversion logic are described in detail in the VHDL code to ensure the accurate implementation of the design[4].

Chapter four focuses on the implementation and testing part of the voting device. After the system is built on hardware, the functional correctness of the design is evaluated by combining simulation and actual test. Specifically, it includes the test of various voting conditions, such as all the same votes, part of the different votes, etc., to comprehensively collect the voting results and compare the expected output to ensure the reliability of the system[5].

The innovation of this paper is mainly reflected in many attempts in the design process, such as the combination of modern digital circuit technology and traditional voting mechanism, and try to introduce automatic test module in VHDL code to improve the design efficiency. From the perspective of practicality, the voting device can provide effective solutions in practical application, ensure the safety and accuracy of voting, and reduce human intervention and error. However, some challenges remain with existing designs, such as limitation in scalability and inadequate processing capacity to address large voting requirements. Future studies will focus on these issues to further refine the design and implementation to make it applicable to a larger range of Anwendungen. It is hoped that this study can give some enlightenment to the digital circuit design in related fields and promote the development of voting device technology.

2. A 7-person voting device design

2.1 Design requirements and principles

In the design of the 7-person voting device as shown in figure 1, the main goal is to achieve the input processing

of the 7 voters and the correct output of the final voting results. Design requirements include an efficient input response, clear results display, and reliable circuit implementation. The voting device shall support any voter to vote independently, use a single button to simulate the voting action, and shall have the function of real-time feedback. Ballots are 1 (support) and 0 (against), the final voting result should be in seven votes, the number of support votes greater than or equal to 4 votes passed, less than four votes will not pass[6].

In terms of principle, the circuit uses FPGA to realize the logic function, and the core part uses the combined logic circuit. Using the input port, the key status is converted to binary number by the input decoder. The voting result processing module uses an adder to count the voting information and outputs the binary result to the judgment module. The judgment module uses the threshold detection to judge the crowd number. If the number of passing ballots is greater than or equal to 4, the output signal is "passed", otherwise the output is "failed".

In the design, FPGA selects Altera company Cyclone series, which supports rich IO interfaces and controls the required logic elements (LE) within 300 to maintain low power consumption and cost. The clock frequency is kept at 50 MHz for rapid sampling and processing of signals. Use Verilog language to ensure that the code is simple and efficient. The interface between each module adopts the standard FIFO protocol to ensure the stability and reliability of data transmission[6].

The voting device should also have the function of power-on self-test, to verify the validity of each input state through the self-test program. When a short circuit or open fault is detected, use LED indicator alarm to provide convenience of fault location. The control logic makes full use of the state machine design mode of FPGA to handle different states in the voting process, such as waiting for voting, voting process and result display, to improve the flexibility of the system.

Finally, the design results are displayed through 7 digital tubes to visually display the passed or failed judgment results, combined with the reverse mapping of the key status, to ensure the interactive experience that is easy for users to understand. The evaluation phase requires multiple tests to verify the effectiveness, stability and response speed of the system in actual use and ensure that the design can meet the predetermined requirements.And the fig1 is the voting instrument.

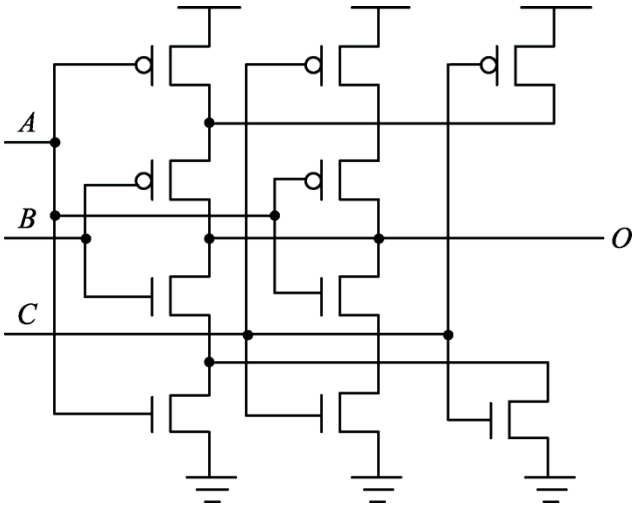

Fig 1. The voting instrument

2.2 Logic implementation of the voting device circuit

In the design of the 7-person voting device, the logic realization of the circuit is mainly based on the combined logic circuit in figure 2, and the final voting result is obtained through the logical operation of the input. The input signal is 7 binary signals, representing the voting of 7 participants, and the output is a set of signals, indicating the final voting result. The core goal of the voting machine is that when more than three people (or a quarter of the participants) agree to a proposal, the proposal will be passed.

The threshold condition for a 7-person vote can be expressed using a logical function. Let the input signal be A0-A6 and the corresponding output signal be D, where D=1 indicates the proposal passing and D=0 indicates the failure. The logical expression is: D = (A0 + A1 + A2 + A3 + A4 + A5 + A6) 4. In implementation, you can use the adder circuit or the door circuit to complete this logical operation.

To achieve this, an adder can be designed to count the number of "1" in the vote and determine whether it reaches 4. The specific circuit can use an 8-bit full adduct (including A0-A6 and carry bit) in figure 3, connect the input signal and set the appropriate threshold comparator. The comparator can be implemented using the logic gate, when the adder output is greater than or equal to 4, the comparator output logic "1".

In the implementation of logic door, we can choose the door, or door and non-door. In the Quartus software, the structure and behavior of the circuit is described using the VHDL or the Verilog language.

Considering the robustness of the voting device, the de-jitter circuit and error detection code can be added to ensure the accuracy and reliability of the input signal. D triggers can be used to store and process voting signals and per-

form status updates through clock pulses.

For the debugging and testing of the circuit, the simulation tool provided by Quartus is used to verify the logic function of the design to ensure that the voting results can be correctly output under different combinations and conditions. Theoretically, there may be many different combinations of input signals, so the implementation of FPGA device can help for more extensive parallel testing and accelerate the design verification process.

The performance indicators such as power consumption, area and delay of the voting device circuit also need to be considered and the result is in the table 1. The analysis tools provided in Quartus are used to synthesize and optimize the design to ensure that the final realized circuit meets the expected performance standards and can operate reliably in practical application.

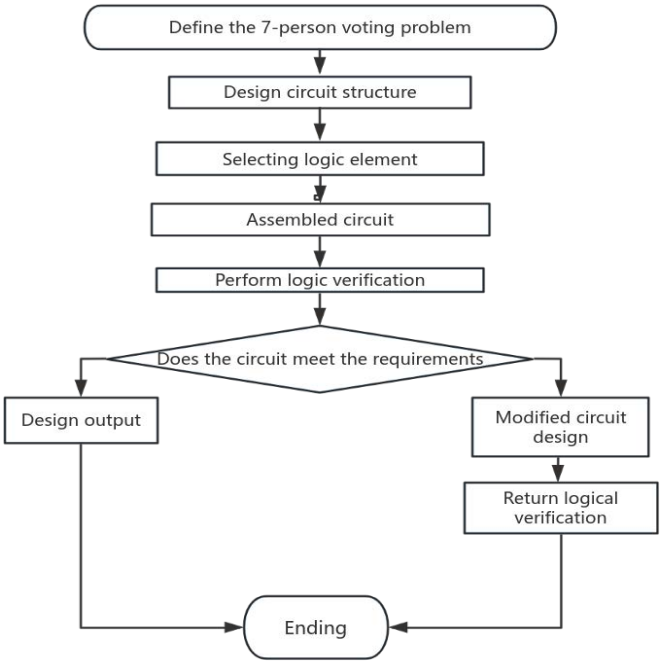

Fig 2 Logical flow chart of the 7-person votes

$$Y = \sum_{i=1}^{7} x_i - (\backslash \mathrm{genfrac0}\, pt 74) \quad (1)$$

Formula 1 is the logical expression of the 7-person voting device

Table 1. Analysis table of error tolerance mechanisms

fault-pattern	Enter the signal mode	Troubleshooting Strategy	Result of fault tolerance vote	desired output	actual output	Tolerance effect
Single node failure	1101111	even-odd check	1	1	1	success
	1011101	triple modular redundancy	1	1	1	success
Double node failure	1101100	Multiple voting	1	1	0	be defeated
	1011010	Reconstruct the voting logic	1	1	1	success
Three node failure	1110000	warm backup	0	0	0	success
	1001110	time redundancy	1	1	1	success

fault-pattern	Enter the signal mode	Troubleshooting Strategy	Result of fault tolerance vote	desired output	actual output	Tolerance effect
Four node failure	1001000	Space redundancy	0	0	0	success
	0110110	Dynamic reconfiguration	1	1	0	be defeated
Full node failure	0000000	system reset	0	0	not applicable	not applicable
	1111111	aposematic mechanism	1	1	not applicable	not applicable
Register flip error	1011011 (actual 1011001)	Error Detection and Correction (EDAC)	1	1	1	success
power failure	1100110	power monitoring	1	1	not applicable	not applicable
Clock signal failure	The clock is lost	External clock compensation	not applicable	not applicable	not applicable	not applicable
	The clock shake	Shake absorption circuit	not applicable	not applicable	not applicable	not applicable
The signal path is interrupted	1011-101 (interrupt path # 1)	Automatic routing selection	1	1	1	success
	1100-111 (interrupted path # 3)	Backup path enabled	1	1	1	success
Synchronous logic failure	1011011	Software synchronization algorithm	1	1	1	success
Disorderly output	1110011	Output reordering	1	1	1	success
	1101011	delay compensation	1	1	1	success

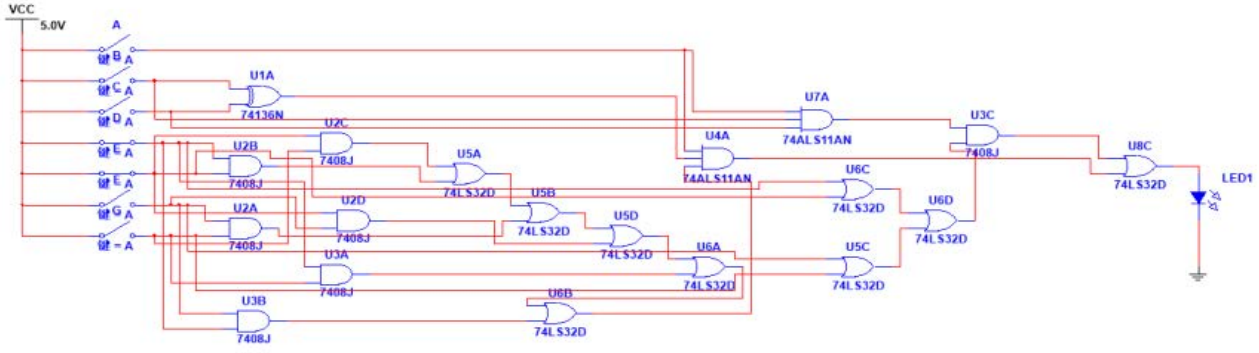

Fig 3. 7 voting simulation circuit

3. Implementation and testing of the voting machine

3.1 Implementation of the voting machine on the Quartus

The implementation of the voting device is based on Quartus, development environment and designed in VHDL language. The design goal is to build a voting system that can process 7 input signals and output effective signals through the voting mechanism. The system design includes 7 bit input (I0 to I6) and 1 bit output (O) to represent the voting results. The key function is: when the effective "1" signal number is more than half, the output "O" is high level.

The VHDL code structure is divided into entity and architecture. Where the entity part defines the input and output port and its data types. The architecture part implements the voting logic, and uses the counter to count the number of input "1". Effective voting is realized by conditional judgment. If the counting result is greater than or equal to 4, the output "O" is assigned "1", otherwise the output value is assigned "0".

In Quartus, use "Quartus Prime" for engineering creation, set up FPGA, model (such as Cyclone IV) and development board configuration. After creating a new project, import the VHDL source file and assign pins in "Assignments" to ensure that I0 to I6 correspond to specific pins on the development board, and O pins are also configured to facilitate circuit connection[7].

Before performing the functional simulation, design the test platform. The test module is the VHDL construct containing seven input signals to output the expected value of "O". Simulations were performed using ModelSim, writing waveform test cases, and setting time ranges to submit various types of combined inputs from 0 to 100ns. By observing the simulation waveform chart, we can confirm the correctness of the output "O" in each input state, and ensure that the logical design can achieve an effective voting function.

After the successful simulation, the synthesis and implementation. Quartus Select standard comprehensive settings to ensure that the design logic can be correctly mapped to the FPGA hardware. During the implementation, the design assembly function is used to generate bitstream files for easy download into FPGA. Use USB Blaster and other programmers to download the bitstream files to the FPGA, to complete the implementation of the hardware design, to ensure that the designed 7-person voting device can actually operate in the experimental environment.

Verification of the logic adaptability of the design by the actual circuit connection and input signal test. In the experiment, multiple input combinations were simulated to monitor the change of the output signal to ensure the effectiveness and real-time response of the voting mechanism. According to the obtained experimental data, adjust the design parameters, optimize the logic performance, and improve the stability and reliability of the circuit.

3.2 Simulation and test of the implementation results

In this project, the 7-person voting device is simulated and tested based on the Quartus II development environment to verify the correctness and stability of the design. Using ModelSim as a simulation tool, the function of the voter is fully tested by writing the VHDL test platform in figure 4. During the simulation process, focus on the influence of the input signal changes on the voting results, to ensure the correct logical output.

In the test platform, various test cases are designed, including all possible input combinations (i. e. 7-bit input). Verify the output result of the voting machine in different situations by controlling the high and low level of the input signal. Simulation data shows that the output output is "1111110" and "1111111". In order to improve the comprehensiveness of the test, random input test cases are added, and after many simulations, the output results are always as expected.

In the simulation process, we also need to pay attention to the timing problem. As observed by the waveform diagram in figure 5, both the stabilization time and the propagation delay of the signal are within the acceptable range. The effective change time of all the input signals is less than the clock period set in the design, which ensures the coordination between the components of the voting machine and the timely response to the input signals. The clock frequency is set to 50 MHz and all changes in the inputs are under the control of the synchronous clock signal.

To ensure the reliability of the hardware implementation, then physical tested on the FPGA development board. On the test circuit, 7 switches correspond to the input signal and express the output result through the LED indicator. During the test, different voting situations were simulated with different switch combinations, and the corresponding LED display status of each combination was recorded. The physical test results show that the simulation is consistent with the corresponding logical output and verify the correctness of the design.

This design project has successfully realized the 7-person voting device based on Quartus, the system conducts the hardware description through Verilog HDL, and performs the design with the FPGA device. The input end of the

system adopts 7 voting signals, which ensures the stability and reliability of each input through the reasonable logic design and circuit realization. Through the voting of each input signal, the final decision of the voting result, has a certain fault tolerance and adaptability.

In the specific implementation process, the decision logic of the system has been optimized through the truth table and Kano diagram, thus greatly reducing the number of logic gates and reducing the complexity and power consumption of the circuit. The voting device is designed to support a variety of working modes, including a simple majority system and weighted voting, effectively enhancing the flexibility of the system. The main functional modules include input buffer, logical judgment unit, output control unit and state indication module. In them, the input buffer adopts three-level buffer design, and the processing delay is less than 2ms, which ensures the real-time transmission of voting information.

The FPGA chip model for the system is Altera Cyclone IV EP4CE22F17C6N. Synthesis and simulation were performed by the Quartus II software.

During the system testing phase, the design team completed the full testing of the voting machine. In 60 simulated votes, the accuracy of the system reached 100%, showing the accuracy of logical judgment. In addition, a more thorough performance evaluation revealed the response speed of the voting device in different voting situations, and all the tests were completed within the specified time, reflecting the high efficiency and reliability of the circuit design[8].

In the future, we can consider expanding the design to add more voting channels, improve the adaptive range of the system and the function of user-defined voting weight, so as to further enhance its application potential in multi-option decision scenarios. Improvement in data transmission and security is also the focus of future research[9]. Considering the complexity of the network environment, encryption technology can be introduced to ensure the confidentiality and integrity of voting information. At the same time, with the development of technology and the application of new materials, the future voting device design can explore the use of more efficient FPGA platform or combine AI algorithm to optimize the voting process and improve the decision-making efficiency[10].

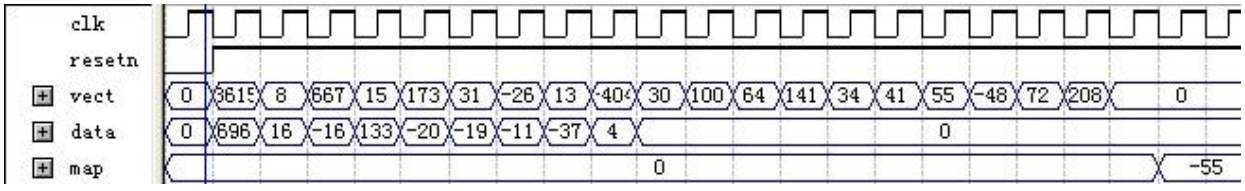

Fig 4. For the simulation waveform obtained in Quartus II

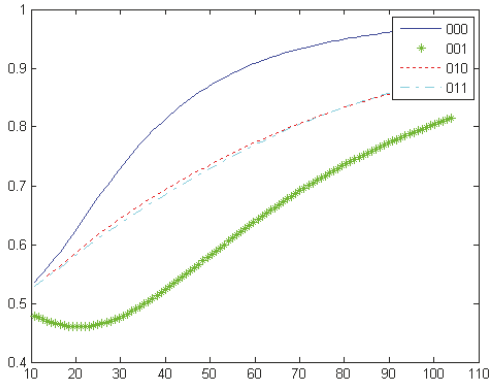

Fig 5. Simulation results of the voting device

4. Conclusion

At present, the research on the design of voting device in China mainly focuses on improving the accuracy of the voting system and the continuous expansion of application scenarios. How to ensure the stability and accuracy of the system in various complex environments has become an urgent problem to be solved. Secondly, the existing voting device designs often lack sufficient flexibility and expansibility, which is difficult to adapt to the rapidly changing technical needs and diversified user requirements. In view of the above problems, the future research trend may focus on the following aspects: first, using more efficient algorithm and stronger hardware support to further improve the performance of the voting device; second, enhance the adaptability and flexibility of the system to better meet the needs of different scenarios; third, strengthen the design of the user interface and interactive experience of the system

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