Dean&Francis

ISSN 2959-6157

Design and Optimization of CMOS Layout Structure

Xuquan Liu[1, *]

[1]School of Engineering, Hong Kong University of Science and Technology, Hong Kong, China

* Email: xliugp@connect.ust.hk

Abstract:

CMOS process is currently the mainstream process technology for large-scale integrated circuits. The integrated circuits manufactured by this process have the advantages of low power consumption and high integration. With the continuous upgrading of semiconductor technology theories and design concepts, CMOS IC layout design is no longer a simple graphic design at the beginning, but has developed into a complex design problem that requires comprehensive consideration of various factors. Therefore, the design of layout and optimization for different problems have become more and more important. In this paper, we summarize the contents of the current mainstream CMOS layout design, common design difficulties and problems, and the optimization solutions proposed for each type of problem. The paper will first introduce the basic rules and fundamental flows of layout design, outlining their definitions and purposes. Secondly, the paper will present the optimization of the layout design taking into account different factors and problems. In particular, it focuses on the improvement schemes of the layout when facing the chip failure problems such as ESD effect and Latch-up effect.

Keywords: CMOS Process; Layout Design; Layout Optimization; Chip Failure.

1. Introduction

1.1 Background and Significance of the Research

With the advent of the data-oriented era, chips have been used in a wide range of people's lives. Whether it is AI large model training at the forefront of science and technology [1], or smartphones and other electronic products used in people's daily life [2], there is no lack of chips. All this comes from the continuous progress of chip manufacturing technology. In the past half century, people have been driven by Moore's law to reduce the feature size of the chip, improve the integration of the chip, and arrange more transistors on a smaller silicon wafer [3]. CMOS (Complementary Metal Oxide Semiconductor) process has become the mainstream large-scale integrated circuit fabrication process for many years with many advantages such as low power consumption,

high integration, high interference immunity, low cost, and so on.

However, as the transistor size decreases, some microscopic physical effects begin to have an increasingly significant impact on the circuit, while the parasitic effects inherent in the CMOS process are also amplified in the small size case. In order to efficiently utilize the space of the chip, while also taking into account the protection against a variety of unfavorable factors affecting the circuit, the layout design has become more and more complex and important from the simple graphic design at the very beginning. In addition to adhering to various basic design principles, special layout design optimization is subsequently required to solve various specific problems in order to ultimately produce competitive chips. How to design a layout that can match the process and how to give effective optimization solutions when facing different influencing factors are questions that must be answered in today's ever-advancing technology.

1.2 Content of Research and Article Structure

This paper summarizes the contents of the current mainstream CMOS layout design, the common design difficulties and problems, and the optimization solutions proposed for each type of problem. In Chapter 2, the paper will first show the basic rules that need to be followed in the current layout design, and the corresponding problems behind these rules. Then, this paper will briefly describe the basic flow of layout design and the problems that need to be focused on in each step. Secondly, in Chapter 3, the paper will present the optimization scheme of layout design under the consideration of different factors and problems, including chip failure problem, parasitic parameter problem, process error problem and noise problem. The focus of this paper is to explain the improvement of the chip failure problem, including the principle of electrostatic discharge effect and latch-up effect, the hazards, and the more effective protection measures. Finally, the full text is summarized in Chapter 4.

2. CMOS Layout Design

2.1 Basic Rules of Layout Design

Although in principle the circuit designer can determine the length and width of each transistor, in order to produce a fully functional and reliable circuit under the existing process conditions, the designer must follow a number of design rules in the actual layout design [4], otherwise the final product will be unsatisfactory. A design rule is a set of rules that basically ensures that the transistor is built and connected correctly regardless of deviations at each step of the fabrication process.

Most design rules can be incorporated into the following four rules: (1) Minimum width: Based on the level of lithography and process, the width of the geometry defined on the mask must be greater than a minimum value. If the width of the metal linkage is too narrow, the metal linkage may be broken or a large resistance may appear locally due to process errors. Usually, the thicker the connecting layer, the greater the minimum allowable width of the layer. (2) Minimum Spacing: On the same mask layer, the spacing between patterns must be greater than a minimum value. In some cases, even different layers of mask graphics spacing must be greater than this minimum value. If the spacing between two polysilicon links is too small, a short circuit may result. If a metal line is too close to the emitter or collector of a transistor, the injection region of the enclosing transistor may overlap with that metal line. (3) Minimum Surround: In the bipolar transistor layout, we mentioned that both the N_{well} and P_{sub} injection regions should have enough margin around the transistor to ensure that the device portion is always inside the injection region, even in the event of process errors. (4) Minimum Extension: Some shapes should be extended at least a minimum length beyond the edges of the other shapes to ensure proper operation of the circuit. For example, to ensure that the base channel resistor can work properly, Emit must have a minimum extension outside the Base area.

2.2 Basic Flow of Layout Design

(1) Delineation of isolation area: According to the principle of isolation area, NPN tube with the same collector potential can be placed in an isolation area, and PNP tube with the same base area potential can be placed in an isolation area. If the collector of the NPN tube and the base of the PNP tube have the same potential, they can also be placed in an isolated area. The placement of resistors is more flexible and can be arranged according to the situation; capacitors occupy a larger area and can be placed in a separate isolation area [5].

(2) Design of component graphics and dimensions: As with the layout design of digital integrated circuits, the graphics and dimensions of the components are designed on the basis of analyzing the circuit and according to the current on each branch and the requirements for component current capacity, voltage withstand, frequency characteristics, etc. [6]. The maximum operating current allowed to flow per unit effective emitter area bar length for small size tubes is limited, and small size transistor graphics with single emitter, single base and single collector can be used. High power tubes have high withstand

ISSN 2959-6157

voltages, can output sufficiently large currents, and have good secondary breakdown performance and large current gain, although they consume more power. In general, the area of the high-power tube can account for more than half of the entire chip area.

(3) Layout and wiring: the layout and wiring of the circuit has a great impact on the yield, the general principle is: (a) strive to compact component arrangement to reduce the impact of parasitic effects and improve yield. (b) the requirement of symmetry of the transistor in addition to ensuring that the graphics should be consistent, its location should also be as close as possible to minimize the adverse effects caused by materials, processes and temperature inhomogeneity. For the requirements of symmetrical resistors should be taken in parallel arrangement to reduce the error caused by lithography, manufacturing process. (c) After accurately analyzing which components in the circuit must maintain strict thermal matching, and understanding the temperature distribution caused by the thermal effect of the power tube, then decide on the layout of the power tube, thermal matching components and other components. iv. The arrangement of the lead-in terminals should be in line with the unified standard of the general-purpose operational amplifiers, and the distribution of the soldering points should be uniform in order to adapt to the different forms of packages.

3. CMOS Layout Optimization

Understanding the rules of layout design is only one of the most basic steps, but also must understand the corresponding circuit design and process knowledge, because mastering this knowledge not only allows the designer to better understand the circuit, but also according to the defects of the process to take the form of layout optimization to make up for, or in the process of layout design in time to find the layout of the potential weaknesses of the protection measures. In this chapter, various factors affecting layout design will be discussed and corresponding layout optimization solutions will be proposed.

3.1 Layout Optimization Solution for Chip Failure Problems

ESD effect and Latch-up effect are two common causes of chip failure [7]. Understanding the principles, hazards and corresponding layout optimization methods of the two can effectively avoid the impact of chip failure problems on chip lifetime.

3.1.1 ESD effect

The full name of ESD is Electronic-Static Discharge. ESD is the transfer of charge between two or more objects with different potentials due to electrostatic induction or direct contact [8]. Three necessary conditions are required to generate ESD: (1) The presence of a source of interference. (2) There are coupling conditions. (3) The presence of sensitive equipment.

Typically, when ESD occurs, the current of the order of amperes is instantaneously released in nanoseconds to microseconds, and the instantaneous power reaches thousands of watts, which is extremely damaging to the chip. When the chip occurs electrostatic discharge, the chip will fail, this failure may be short-lived, or may be permanent. There are three kinds of ESD failure: (1) Hard failure: material damage or destruction, cannot be recovered. (2) Soft failure: temporary change of logic function, the possibility of recovery. (3) Latent failure: temporal failure, the occurrence of failure or not with time random change. No matter what kind of failure, in the design should be avoided, it will directly affect the reliability of the chip.

ESD protection circuit can reduce the possibility of working circuits become ESD discharge path, to avoid working circuits are damaged by ESD. ESD protection circuit works to ensure that ESD occurs between any two pins, there is at least one low impedance bypass, on the one hand, can absorb ESD current, on the other hand, can clamp the operating voltage, to prevent damage to working circuits due to large operating voltage.

In CMOS process, gate-grounded NMOS tubes (GGNMOS) are often used as ESD protection devices. In the event of ESD, the GGNMOS can utilize the snapback effect to clamp the transient high voltage and discharge the current. The advantages of this conduction mode are low clamping voltage and low on-resistance. When a pulse is introduced at the PAD (chip pin), the drain is reverse biased by the voltage and the GGNMOS enters the “high-resistance region” until the device undergoes a breakdown. As the substrate voltage rises, when it reaches enough to make the parasitic bipolar NPN tube open, the GGNMOS into the “differential negative resistance area”, at this time the device can uniformly absorb the large current generated by the ESD, and play a very good role in ESD protection. However, it should be noted that if the current continues to rise, GGNMOS into the “negative resistance effect area”, the device will produce a localized “hot spot”, and once again breakdown occurs (Figure 1).

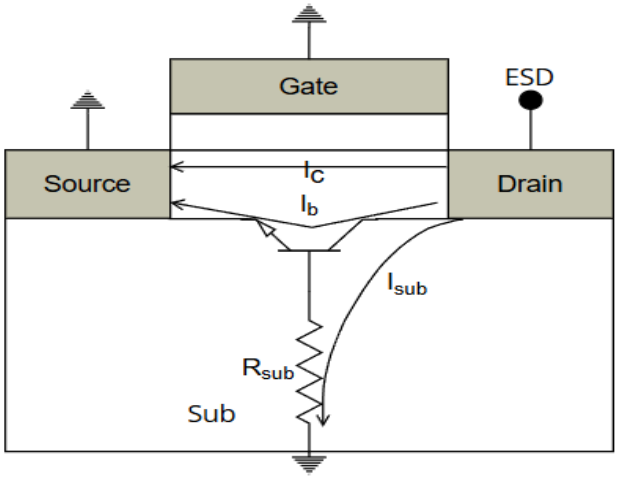

Fig. 1 GGNMOS and parasitic NPN structure diagrams

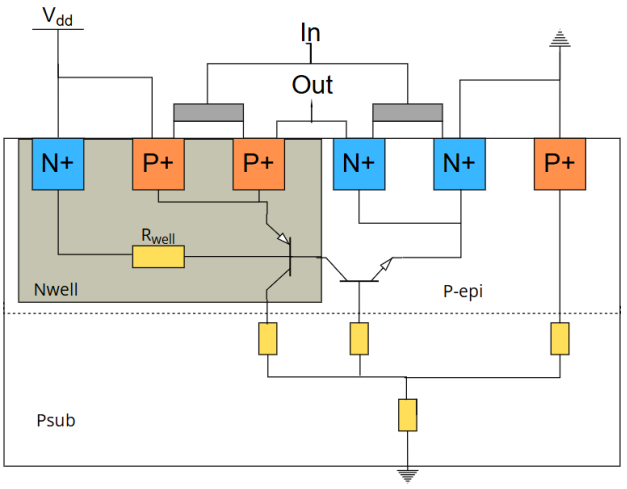

Fig. 2 Profile of Latch-up

To further enhance the circuit's resistance to ESD, the following two approaches can be used [9]:

(1) Expanding the DCGS (drain contact to gate spacing) of the layout ESD device (GGNMOS). The diffusion of the GGNMOS itself is utilized, which is equivalent to an NSD resistor. When ESD occurs, the low impedance path not only absorbs the ESD current, but the operating voltage can also be clamped.

(2) Add Salicide Blocking process. This process is to define an additional Salicide mask. When the process is in production, the area with Salicide is not metallized, and the rest of the area is metallized, so that the resistance of the device source, drain, and gate squares are restored to their original values. The electrostatic discharge through the large resistor generates a large voltage drop, and at the same time reduces the current to achieve the purpose of improving the ESD protection capability.

3.1.2 Latch-up effect

Latch-up is a low-resistance path generated by the interaction of a bipolar PNP and a bipolar NPN parasitized between VDD and GND in a CMOS circuit [10], which usually generates high currents. When the two transistors are in the cut-off state, when the two bipolar devices are relatively small loop gain, does not occur Latch-up. when one of the transistors is disturbed by the current increases to a certain value, it will be fed back to the other transistor, the two transistors successively triggered and then on, so the formation of a low-resistance path between VDD and GND, resulting in a Latch-up (Figure 2).

With the increasing integration of ICs, the impact of CMOS process parasitic effects on the chip becomes more and more obvious, and the chances of generating Latch-up are also increasing, and preventing Latch-up has also become an important task in layout optimization. The following three methods are usually used to prevent Latch-up [11]:

(1) Keep the distance between NMOS and PMOS large enough, and let the Sub contact holes as close as possible to the NMOS away from the PMOS, and the Well contact holes as close as possible to the PMOS away from the NMOS. it is best to let the two kinds of contact holes can be surrounded by a ring, in order to play the role of reducing the R_{well}, R_{sub}. Also try to thicken the power and ground lines in the layout. This type of protection is most widely used in layout optimization.

(2) Adding Guard Ring The addition of Guard Ring not only prevents the latch-up effect, but also isolates the noise, which is often used in the actual layout design. There are two main types of Guard Ring: (a) Majority Guard Ring works by lowering the resistance of R_{well} and R_{sub}. P_{sub} surrounds the NMOS as much as possible in a ring around the GND potential, and N_{well} surrounds the PMOS as much as possible in a ring around the VDD potential. (b) The principle of the Minority Guard Ring is to minimize the amount of minority carriers injected into the Sub or Well, thus reducing the possibility of a Latch-up. P_{sub} surrounds the PMOS and its own N_{well} as much as possible in a ring around the GND level, and N_{well} surrounds the NMOS and its own P_{sub} as much as possible in a ring around the VDD level.

It is important to note that the term Majority is relative to the term Minority. For a PMOS transistor, N_{well} is the Majority Guard Ring and P_{sub} is the Minority Guard Ring, whereas for an NMOS transistor, the opposite is true.

(3) Independent double-well protection. This layout is

ISSN 2959-6157

probably the best of the three in terms of anti-Latch-up effect. The triple-well structure completely blocks the coupling between the NMOS protection circuit's parasitic NPN and the substrate. Due to the existence of two independent traps, the distance between the parasitic NPN and the PNP is widened on one hand, and the coupling between the PNP and the NPN is eliminated on the other hand, which destroys the mutual feedback structure between the PNP and the NPN, and thus inhibits the formation of Latch-up.

3.2 Layout Optimization Solution for Parasitic Parameter Problems

Process layers are an important part of chip design. Whenever two different process layers are introduced in process fabrication, corresponding parasitic devices are created [12], which are widely distributed throughout the chip and cannot be eliminated. Parasitic devices are very undesirable for the designer, they can slow down the circuit, change the frequency response or cause some unexpected things to happen. Because parasitic devices cannot be avoided, only through the optimization of the design to minimize the impact of parasitic parameters. Parasitic parameters mainly include the electrical parasitic capacitance and parasitic inductance.

Reduce the parasitic capacitance can start from the following aspects: (1) wire length. The most direct way to reduce the parasitic parameters is to minimize the length of the wire, because if the wire length is small, the capacitance generated by interaction with it, such as the capacitance of the metal or substrate layer, will be reduced accordingly. (2) Selection of metal layer. The main parasitic capacitance is usually the capacitance between the wire and the substrate. By changing the metal layer, the generation of this capacitance can be reduced. Since the magnitude of the capacitance is inversely proportional to the spacing of the plates, a little change in distance can cause a big difference. (3) Metal overlay. In the automatic layout wiring often occurs when wiring on certain circuits, the layers of metal overlap often produce significant parasitic capacitance. It is best to artificially separate the sensitive signals, try to avoid the sensitive circuit above the line, but let the metal line in between the circuit, so that the parasitic parameters are small and relatively easy to control.

The solution to parasitic inductance is to treat it as an integral part of the circuit (because it will always be there). After completing the layout, estimate the inductance that may be induced in each part of the circuit, taking care not to allow inductive coupling to affect the rest of the circuit.

3.3 Layout Optimization Solution for Process Error Problems

The dimensions of the pattern produced on a silicon wafer will not be exactly the same as the dimensions of the layout because the pattern shrinks or changes during photolithography, etching, diffusion, and ion implantation [13]. Considering these errors and evaluating their impact on the circuit is an essential part of circuit design.

Several approaches are usually used to minimize the impact of process errors: (1) Selecting devices with lower errors. After the integrated circuit components are manufactured, their parameters will always have different degrees of error, and different devices for the process is not the same degree of dependence. When the circuit requirements are high, it is quite necessary to select devices that depend less on process variation, i.e., higher accuracy. (2) Matching. Most of the integrated resistor-capacitor has an error of ± 20% to 30%, but through matching techniques, the ratio of two similar devices in the same integrated circuit can be better than ± 1%. Increase the basic methods of matching are: finger-crossing devices, common center, four-way cross and other matching techniques. (3) Increase the size of the device. For multiple devices that match each other, increasing their size can make their matching degree higher. At the same time, the use of large-sized devices also has other benefits, such as reducing device noise. However, the pursuit of using large-sized devices will result in wasted chip area and larger parasitic parameters, which will not be worthwhile in the end.

3.4 Layout Optimization Solution for Noise Problems

As the precision of integrated circuits continues to improve and the speed of circuits gradually increases, the noise generated by circuits with high-speed actions and the white noise generated by various circuit components fill the entire chip. It is an important issue to be able to make the key parts of the circuit as well as the high-precision modules precisely fulfill the required functions without being interfered by the noise.

The following ideas are provided to effectively ameliorate the effects of noise: (1) Adequate ground shielding. The substrate of the chip is spread all over the place and once the noise is present on the substrate, it will propagate to every part of the chip. So the designer should take a variety of techniques to make the noise does not enter the substrate. Simple and effective method is to put a lot of noise around the device on the substrate contact, these enough number of contacts can effectively prevent the noise into the substrate. (2) Reasonable layout. Separate the noise-generating parts of the circuit from the circuits that require high-precision work, and separately add ex-

cellent shielding to these parts, such as connecting a specific potential of the protection ring, which can minimize the impact of noise on the critical circuits. (3) Coupling of input and output ports. For each module, if the inputs and outputs are too close together, the output signals will affect the input circuits through parasitic coupling. Therefore, consideration must be given to placing the inputs and outputs of the circuit farther apart to avoid coupling affecting the normal operation of the circuit. (4) Increase the size of the device. Increasing the size of the device can reduce the noise generated by the device, but as mentioned above, increasing the size of the device will bring a series of problems such as increased chip area, and therefore need to be considered as a compromise.

4. Summary

This paper summarizes the four basic rules of CMOS process layout design and the three basic steps of the design flow, according to which the designed chip can be well compatible with the current process level and ensure a good yield. Subsequently, this paper puts forward layout optimization solutions for the common problems affecting circuits one by one, including chip failure, parasitic parameters, process errors, noise interference and other problems. For the chip failure caused by ESD effect and Latch-up effect is analyzed in detail and put forward a variety of improvement measures based on the existing program. Many optimization ideas are also proposed for technical parameters, process errors, noise interference and other problems. After optimizing the layout for different design problems of the chip, the chip can not only make up for the defects of the process level to a certain extent, but also play a better performance and have a longer service life in a specific working environment.

However, the current use of CMOS process chip layout design is still a balancing act: if we need to meet a number of indicators on a chip at the same time, it is inevitable to tolerate some of the less important indicators become bad; if we want to make the chip in a certain aspect of the chip has excellent performance, we need to be ready to pay a high cost of preparation for this. For example, when dealing with noise problems, whether to increase the size of some devices to achieve the effect of noise reduction needs to be carefully considered. Or in order to reduce the interaction between the metal to increase the spacing of the wiring, space utilization will be worse to a certain extent. In short, under the current technology, the layout design still needs to make reasonable trade-offs, so as to achieve a satisfactory degree.

References

[1] Kim Taepyeong, Park Sangun, Cho Yongbeom. Study on the Implementation of a Simple and Effective Memory System for an AI Chip [J]. Electronics, Volume 10, Issue 12, 2021, PP 1399-1399.Fangfang. Research on power load forecasting based on Improved BP neural network. Harbin Institute of Technology, 2011.

[2] Terashima T, Yamamoto F, Hatasako K, Hine S. 120V BiC-DMOS process for the latest automotive and display applications [C]. Power Semiconductor Devices and ICs, 2002, Proceedings of the 14th International Symposium on 4-7 June 2002:93~96.

[3] Paulr Gray, Paulj Hurst, Robert G. Meyer. Analysis and Design of Analog Integrated Circuits [M]. Higher Education Pres, 2003.

[4] Da Feifei. Research and Design of a Step-down DC/DC Converter [D]. Xi'an University of Electronic Science and Technology, 2009.

[5] Phillip E.Allen, Douglas RHolberg. CMOS Analog Circuit Design Second Edition [M].Beijing: Publishing House of Electronics Industry, 2005.

[6] Yu Qianwei. Design of Single-chip Multi-function DC/DC Converter [D]. Xi'an University of Electronic Science and Technology, 2011.

[7] Zhu Yuezhen. Study of Chip Layout Design Technology and It's Optimization [D]. Suzhou University, 2014.

[8] Young Gu Kang, Hyeon Do Park, Hyun Sung Park, et al. A Study on the Optimal Design of ESD Protection Circuit in OLED Panel Using Electromagnetic Simulation [J]. SID Symposium Digest of Technical Papers, Volume 55, Issue 1, 2024, PP 1203-1206.

[9] Boyang Ma, Shupeng Chen, Ruibo Chen, et al. Deep n-well dtscr with fast turn-on speed for low-voltage esd protection applications [J]. Microelectronics Reliability, Volume 160, 2024, PP 115475-115475.

[10] Milova Paul, B. Sampath Kumar, Harald Gossner, et al. Engineering Schemes for Bulk FinFET to Simultaneously Improve ESD/Latch-Up Behavior and Hot Carrier Reliability [J]. IEEE Transactions on Electron Devices, Volume PP, Issue 99, 2020, PP 1-7.

[11] Ruibin Li, Chaohui He, Wei Chen, et al. Impact of TID on latch up induced by pulsed irradiation in CMOS circuits [J]. Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms, Volume 440, 2019, PP 95-100.

[12] Zhang Yanyan. Analysis of a Monolithic Buck DC-DC Converter Chip and Optimal Design of Its Layout [D]. Xi'an University of Electronic Science and Technology, 2012.

[13] RJocob Baker, Harry W Li. CMOS Circuit Simulation and Layout Design [M]. China Machine Press, 2003.