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ISSN 2959-6157

Design of Low Power Integrated Circuits

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Abstract:

The rapid development of integrated circuit technology has made the design of low-power circuits a major concern in this field. Power consumption limits the prolonged operation of high-performance computer systems, affects system performance and heat dissipation, and shortens the operating lifespan of portable devices. The fundamental causes of power consumption, including static, short-circuit, and dynamic power consumption, are thoroughly examined in this work, which focuses on the design of low-power digital integrated circuits. Power and voltage designs, DVFS (dynamic voltage and frequency scaling), and closed-loop clocking are some of the tactics for implementing low-power technologies that are also discussed. In addition, new ultra-low power designs such as field-effect transistors (FETs), semiconductor organic integrated circuits (SOIs), and tunneling field effect transistors (TFETs) are shown, and their usefulness is shown by way of an example of a Bluetooth 5.0 system-on-chip (SoC) application. Future developments in low-power design will guarantee ongoing innovation in high-performance electronic systems by optimizing device layouts and making use of new materials.

Keywords: Low Power Design; Power Optimization; Finfet; Dynamic Voltage Scaling (DVFS).

1 Introduction

In recent decades, the swift advancement of integrated circuit process technology has led to substantial improvements in the processing speed and integration density of digital integrated circuits. As device sizes diminish, power consumption progressively constrains the performance enhancement of integrated circuits. Power consumption influences both the system's overall performance and stability, as well as significantly affecting heat dissipation and energy efficiency of the device. In sectors like smartphones, IoT devices, and portable electronics, low-power design has emerged as a crucial element for enabling prolonged device operation, enhancing user experience, and minimizing energy usage. Consequently, low-power design is very critical in contemporary digital integrated circuit design.

Typically, digital integrated circuits' power consumption is broken down into three categories: dynamic, static, and short-circuit. When both PMOS and NMOS transistors are in operation at the same time, transient currents generate dynamic power consumption from capacitor charging and discharging during circuit transitions and short-circuit power consumption from transient currents. Leakage current is the

main cause of static power consumption; this is particularly true with nanometer-scale technologies, where shrinking device dimensions greatly increase static power consumption. Consequently, one of the main challenges in integrated circuit design is to guarantee performance while substantially minimizing power consumption.

This paper offers a thorough examination of low-energy design methodologies and systematically evaluates strategies to enhance energy efficiency across various design tiers (i.e., device architecture, design methodologies, and practical implementations). Initially, the fundamental principles of low-energy design are presented, followed by an in-depth analysis of primary energy consumption sources in integrated circuits and various optimization techniques. Subsequently, many creative architectures for ultra-low-power devices are examined, and three design strategies are presented. The viability and efficacy of these low-power designs are examined through actual applications.

The document is structured as follows: Chapter 1 serves as an introduction, outlining the research's background and significance, as well as the paper's substance and organization. Chapter 2 examines the origins of power consumption in CMOS circuits and analyzes the causes and effects of dynamic, short-circuit, and static power consumption. Chapter 3 elucidates the fundamental principles of low-power digital integrated circuit design and delineates methods for minimizing power consumption through the optimization of circuit architectures, algorithms, and device configurations. Chapter 4 offers a comprehensive overview of the device architectures of ultra-low-power integrated circuits, emphasizing the technical concepts and benefits of novel low-power devices such as FinFET, SOI, and TFET. Chapter 5 presents three low-power design methodologies: multi-power supply and multi-voltage design, dynamic voltage and frequency scaling (DVFS), and gated clock technology, including their implementation techniques and applications. Chapter 6 examines the use of energy-efficient architecture in Bluetooth 5.0 SoC chips and its optimization impact through real applications. Chapter 7 presents advanced technologies for novel low-power designs, including FinFET and GAA transistor technologies, near-threshold computing (NTC), and examines their potential applications in forthcoming low-power designs. Chapter 8 offers a synthesis and perspective for the entire document, delineating the research findings and suggesting avenues for future inquiry.

2 Basic Principles of Low-Power Digital Integrated Circuit Design

System performance, thermal management, and reliability are all heavily impacted by power consumption in digital integrated circuit design. Power consumption may be categorized into three primary sources: dynamic power consumption, static power consumption caused by short circuits, and total power consumption. Power consumption during state transitions in a circuit is caused by the charging and discharging of capacitors. The short-circuit power consumption happens when the PMOS and NMOS transistors are both switched on simultaneously because of transient currents. Even when the circuit is not in use, leakage current continues to use power. The four factors that significantly affect dynamic power consumption are the following: operating frequency, switching activity, load capacitance, and supply voltage. Consequently, you can aid dynamic power usage by lowering the supply voltage. Designers will need to consider both power consumption and performance while deciding whether to reduce the voltage. As device dimensions decrease, static power consumption becomes more important. This is especially true at the nanoscale, where leakage current increases at a rapid rate. The concept of low-power design revolves around reducing power consumption without compromising performance through the use of updated algorithms, refined device designs, and enhanced circuit designs [1].

3 Power Consumption Sources of CMOS Circuits

3.1 Classification of Power Consumption In CMOS Circuits

Three main types of power consumption—dynamic, static, and leaky—make up CMOS circuit power consumption. You can see how they are categorized in Figure 1. Power lost by the circuit as a result of charging and discharging the load capacitance is known as dynamic power consumption. This happens while the circuit is changing states. It is closely associated with the supply voltage, load capacitance, operating frequency, and switching activity. The power used by the transient current and short-circuit power consumption are both components of dynamic power consumption. The former happens most often when PMOS and NMOS transistors are momentarily turned on at the same time during switching. Among the components of dynamic power consumption, short-circuit power consumption stands out in high-frequency circuits [2].

Static power consumption predominantly results from leakage current, which has become increasingly critical in deep submicron processes. As device dimensions diminish, leakage current increasingly becomes the principal factor influencing power consumption. Leakage power consumption is classified into PN junction reverse leakage, subthreshold leakage, gate leakage, and channel leak-

ISSN 2959-6157

age. Each type contributes differently to overall power consumption across various conditions.

Here is how a CMOS circuit's overall power consumption is expressed:

$$P = P_D + P_{SC} + P_S = \alpha C_L V_{DD}^2 f + I_{SC} V_{DD} + I_{leak} V_{DD} \quad (1)$$

where P_D denotes dynamic power consumption, P_{SC} signifies short-circuit power consumption, and P_S indicates static power consumption. Capacitor charging and discharging causes dynamic power consumption, whereas PMOS and NMOS transistors conduction during raising or lowering edges causes short-circuit power consumption. Static power consumption results from the device's leakage current, encompassing subthreshold leakage current, gate-tunnel current, and PN junction reverse current [3].

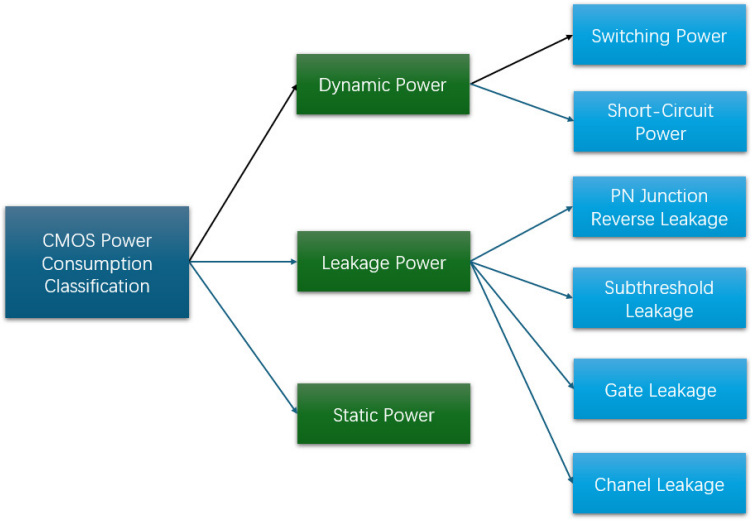

Fig. 1 Classification of power consumption in CMOS circuits

3.2 Dynamic Power Consumption

With most of the power loss in complementary metal-oxide semiconductor (CMOS) circuits occurring during switching due to the dynamics of capacitor charging and discharging, dynamic power consumption best describes the situation. The amount of the load capacitance, the operating frequency, and the supply voltage are the primary variables that impact dynamic power consumption. Common methods for reducing dynamic power consumption include lowering the clock frequency, decreasing the supply voltage, and limiting needless signal switching. One crucial method for lowering dynamic power use is clock gating technology, since it significantly lowers the frequency of capacitor charging and discharging by suppressing unnecessary clock signals. In large-scale integrated circuit design, clock gating technology substantially reduces dynamic power usage. Reducing the supply voltage is an efficient technique to reduce dynamic power consumption. This is because dynamic power consumption is directly connected to the square of the supply voltage.

3.3 Static Power Consumption

The device's leakage current is the primary source of static power consumption. Leakage current grows exponentially with shrinking CMOS devices, which causes static power consumption to gradually increase relative to total power consumption. One typical way to lessen static power usage is by using devices with a high threshold voltage or multi-threshold CMOS (MTCMOS) technology.

Furthermore, innovative device topologies, such as double-gate and multi-gate devices, can significantly reduce static power consumption. These architectures can effectively reduce subthreshold leakage currents through enhanced channel management, rendering them especially suitable for circuit designs at deep submicron and nanoscale dimensions.

4 Device Structures for Ultra-Low-Power Integrated Circuits.

As integrated circuit technology advances towards deep submicron and nanoscale process nodes, the limitations of traditional CMOS devices in terms of power consumption and efficiency are becoming increasingly apparent. To tackle these difficulties, industry and academics have created various new device architectures designed to minimize power consumption and enhance the performance of integrated circuits. Ultra-low-power device architec-

tures exhibit significant promise for optimizing power consumption and serve as a basis for the development of future high-performance low-power systems. This analysis will examine various contemporary and potentially prevalent ultra-low-power device architectures, along with their implementation techniques and benefits.

FinFET technology, a significant advancement in low-power integrated circuit design, has been extensively implemented in advanced technologies of 22nm and smaller. Compared with the traditional planar CMOS structure, FinFET enhances the control of the channel through a multi-gate structure, thereby effectively reducing the subthreshold leakage current. The subthreshold leakage current is the primary contributor to static power consumption in deep submicron processes. FinFET diminishes static power consumption by lowering leakage current and enhances circuit switching speed, consequently augmenting overall performance. In addition, FinFET can operate stably at lower supply voltages, further reducing dynamic power consumption. FinFETs have become the dominant device structure in current advanced node technologies, especially in 16nm and 7nm process technologies, driving low-power designs in mobile devices and high-performance computing [4].

Subsequently, silicon-on-insulator (SOI) technology, as an additional ultra-low-power device architecture, significantly contributes to low-power integrated circuit design. SOI effectively reduces parasitic capacitance and dynamic power consumption by adding an insulator (usually silicon dioxide) between the active region of the transistor and the substrate. In addition, this insulating layer can also block leakage currents from the substrate to the source and drain, significantly reducing static power consumption. Compared with traditional bulk silicon processes, SOI technology can provide similar performance at lower voltages, and its circuits are faster and consume less power [5-6].

In recent years, the tunnel field effect transistor (TFET) has emerged as a promising new device structure with broad prospects for ultra-low power consumption designs. Unlike traditional MOSFETs, which conduct through thermionic emission, TFETs rely on the quantum tunneling effect to conduct by tunneling electrons between the source and drain regions. This allows TFETs to operate at very low voltages and their subthreshold swing can theoretically exceed the 60mV/dec limit of traditional MOSFETs, resulting in extremely low power consumption at low voltages [7].

5 Three Main Methods of Low-Power Design

5.1 Multi-Supply Multi-Voltage Design

The fundamental concept of multi-supply multi-voltage design is to deliver varying voltages to distinct circuit modules to enhance power efficiency while preserving performance. Due to varying performance and power consumption requirements across different modules, numerous power domains are established during design, with each domain configured to supply distinct voltages based on unique demands. This design approach not only efficiently diminishes static power usage but also markedly decreases dynamic power consumption [8].

This design methodology typically depends on a power management unit (PMU) to oversee and control the power states of the different modules. Consequently, non-essential modules can be deactivated or transitioned into a low-power state when inactive, thereby minimizing leakage currents. Power gating is essential in multi-supply, multi-voltage designs, as it mitigates power loss by severing the power supply to inactive modules. This method can conserve substantial energy, particularly in situations characterized by little standby power usage.

While multi-power supply and multi-voltage systems can markedly decrease power consumption, their implementation is intricate, and issues frequently arise in synchronizing timing across many power domains. Consequently, designers frequently depend on standardized low-power design methodologies, such as Synopsys' UPF or Cadence's CPF tools, and employ electronic design automation (EDA) tools to validate power switching and timing.

5.2 Dynamic Voltage and Frequency Scaling (DVFS)

Dynamic voltage and frequency scaling (DVFS) is a method that adjusts voltage and processor frequency based on variations in system load. Under low system load, power consumption decreases by lowering voltage and frequency; in contrast, when the load increases, voltage and frequency are elevated to sustain performance. This method is widely employed in CPUs, mobile devices, and embedded systems to improve energy efficiency and extend battery longevity.

The execution of DVFS necessitates meticulous collaboration between hardware and software. The hardware component enables the modulation of voltage and frequency, whereas the software oversees the system load in real time via the operating system and implements necessary adjustments accordingly. The technology minimizes power usage during low loads while sustaining performance levels under high loads. The efficacy of DVFS is constrained by

ISSN 2959-6157

the regulation's speed and amplitude; thus, it is essential to balance performance needs with power consumption optimization throughout the design phase. While DVFS is an established energy management strategy capable of dynamically modulating power consumption to accommodate varying load conditions, it is not without its challenges. A sluggish adjustment speed may result in a delayed system response, whereas an overly broad adjustment range could compromise system stability.

5.3 Gated Clock Technology

The frequency, distribution and management strategy of clock signals have a significant impact on power consumption in digital circuits. Gated clock technology reduces power consumption by switching off unnecessary clock signals and reducing unnecessary switching. This technology is particularly suitable for modules with frequent switching, such as registers and timing circuits. By switching off unnecessary clock signals, the charging and discharging of capacitors can be effectively reduced, thereby greatly reducing dynamic power consumption.

Typically, gated clock technology uses a multi-level gating scheme to further optimize power consumption. A gated unit can manage multiple subordinate units to form a hierarchical clock management architecture, which can precisely control the transmission path of the clock signal and thereby reduce the power consumption of the global clock tree. In modern large-scale integrated circuit designs, clock gating technology can help reduce dynamic power consumption by 30% to 40% [10-13].

In this technique, selecting the appropriate device threshold voltage (VT) is critical to power optimization. Fig. 2 shows the relationship between leakage current and delay at different threshold voltages (LVT, SVT, HVT) [14]. As the threshold voltage increases, the leakage current decreases significantly, while the delay increases correspondingly. Therefore, the design needs to find an optimal balance between reducing power consumption and maintaining circuit performance. For example, low threshold voltages (LVT) are often used in high-performance blocks to reduce delay, while high threshold voltages (HVT) are used in non-critical path blocks to significantly reduce static power consumption. By combining a hierarchical design strategy with gated clocking techniques, overall energy efficiency can be improved, especially by minimizing dynamic power consumption while maintaining circuit speed and reliability.

Although gated clocking techniques are very effective in reducing power consumption, the timing delay they introduce needs to be carefully managed. Therefore, the design should ensure that the timing constraints remain intact. In addition, although multi-level gated designs can effectively reduce power consumption, they increase the complexity of the design, so a reasonable compromise between power consumption and performance needs to be found.

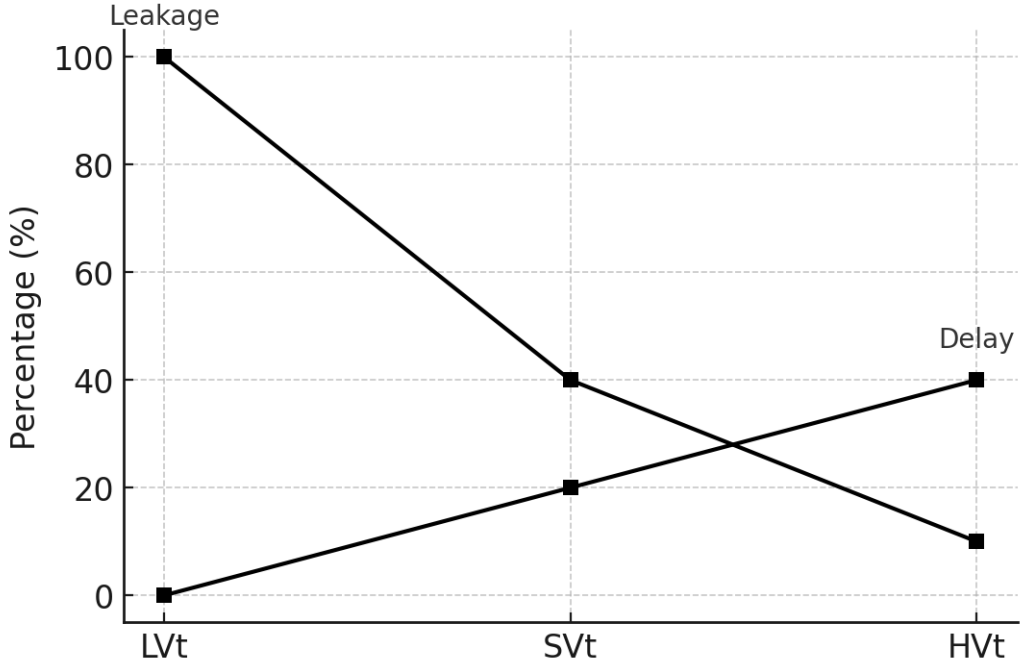

Fig. 2 The effect of threshold voltage (Vt) on leakage current and delay

6 Application Example of Low-Power Design

To ascertain the genuine efficacy of the low-power design techniques, a representative application case is shown for the Bluetooth 5.0 SoC chip design [15]. The chip design employs a multi-power supply and multi-voltage architecture, dynamic voltage and frequency scaling (DVFS), through careful division of power domains and improved clock signal management, as well as gated clock technology, an ideal balance between performance and power consumption may be achieved.

The SoC chip segregates the CPU core, memory, and peripheral devices into distinct power domains using a multi-power supply and multi-voltage architecture, supplying appropriate power voltages based on their specific operational needs. Under elevated load situations, the processor core utilizes a greater power supply voltage, whereas the peripheral devices operate at a lower voltage to enhance energy efficiency. The chip employs DVFS technology to automatically decrease voltage and frequency during low system load to minimize power consumption; conversely, it increases voltage and frequency when high performance is necessary to maintain optimal functionality.

7 Cutting-Edge Technologies and Applications of New Low-Power Design

7.1 Finfet and GAA Transistor Technology

FinFET (fin field-effect transistor) technology has become one of the mainstream low-power design technologies in deep submicron processes [16]. Compared with traditional planar transistors, FinFETs have better channel control capabilities and can effectively reduce leakage currents. FinFETs increase the number of gates of the transistor to enhance the control of current, thereby reducing subthreshold leakage currents, especially at low voltages. FinFET is therefore widely used in processes of 16nm and below and is one of the key technologies for improving power efficiency.

Another technology that can replace FinFET is GAA (gate-all-around), which further enhances control of the channel and can even operate at lower voltages, thereby significantly reducing power consumption. The design of GAA features a gate surrounding all four sides of the transistor, which improves control of the current and effectively reduces leakage current. Therefore, GAA transistor technology has become the preferred solution for nodes of 3 nm and below and is gradually replacing FinFET in high-performance and low-power applications.

7.2 Near-Threshold Computing (NTC)

Near-threshold computing (NTC) is a contemporary low-power design methodology that has developed in recent years. NTC markedly decreases power consumption by modulating the supply voltage to a level around the device's threshold voltage, hence substantially lowering power usage. The NTC principle aims to minimize voltage while maintaining performance integrity. While lowering the voltage may lead to diminished circuit speed, employing parallel processing and modifying the circuit architecture might facilitate a balance between performance and power consumption. NTC technology is extensively utilized in IoT and wearable devices due to their heightened sensitivity to power consumption and less dependence on high computational capability. Utilizing NTC technology, these devices can markedly prolong battery life while attaining an optimal equilibrium between power consumption and performance.

8 Conclusion

With an emphasis on static, idle, and dynamic power consumption, this study examines the main design strategies for low-power digital integrated circuits. Additionally, it suggests ways to optimize power consumption, including clock gating, dynamic voltage and frequency scaling (DVFS), and multi-supply multi-voltage architecture. Research demonstrates that reducing power consumption requires more than simply decreasing supply voltage or frequency; it also necessitates a comprehensive strategy to balance circuit performance with power utilization.

Capacities are charged and discharged most often, which results in dynamic power usage; thus, lowering the supply voltage and minimizing superfluous signal switching constitutes an efficient strategy for reducing dynamic power consumption. Simultaneously, as CMOS technology progressively evolves to the nanoscale scale, static power consumption is escalating rapidly and has emerged as the primary determinant of overall power consumption. Consequently, it is essential to employ high-threshold voltage devices and multi-threshold CMOS technology, which can significantly diminish leakage current without compromising performance.

The low-power design methodologies presented in this study have been validated through practical applications. The Bluetooth 5.0 SoC architecture achieves a balance between power consumption and performance by multi-power supply, multi-voltage design, and DVFS technology. Empirical measurement outcomes indicate that these methods can substantially diminish the total

ISSN 2959-6157

power consumption of the chip, prolong the device's lifespan, and maintain performance. The ongoing advancement of integrated circuit technology has become low-power design a crucial element in the sustainable development of high-performance electronic systems. Subsequent research must persist in enhancing current technologies and investigating novel materials and design strategies to satisfy progressively rigorous power consumption and performance standards.

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