Dean&Francis

ISSN 2959-6157

Enhancing Hand-Written Number Classification with Dedicated Hardware Neural Networks

Yuqi He

College of Engineering, University of California, Davis, The United State

Ukihe@ucdavis.edu

Abstract:

This article explores the integration of hardware neural networks and very-large-scale integration (VLSI) for enhancing the classification and recognition of handwritten numbers, crucial for applications in sectors such as banking and express delivery. Utilizing the perceptron model, the study innovates on traditional methodologies by implementing a hardware-based approach to process weighted inputs through a nonlinear activation function, notably accelerating computation speeds. The perceptron, designed using Verilog, operates within a parallel pipeline tree structure, optimizing the classification process by simultaneously handling multiple data streams, comprising 256 multipliers and 255 adders. This configuration significantly reduces computation time, achieving recognition within 330 clock cycles for each digit, hence establishing a robust foundation for future advancements in machine learning and digital text processing. The research demonstrates that deploying deep learning capabilities directly onto hardware platforms can considerably enhance the efficiency and accuracy of handwritten digit recognition systems, suggesting potential for broader application across various digital interfaces.

Keywords: Handwritten digit recognition; hardware neural networks; parallel pipeline structure.

1. Introduction

In the digital era, the transformation from handwritten manuscripts to electronic formats has become increasingly prevalent across various industries due to the convenience offered by the Internet. This transformation is particularly essential in sectors such as banking and express delivery, where the accurate and rapid classification of handwritten texts is critical. The traditional methods of text recognition are not sufficiently robust to handle the variability and complexity of handwritten digits efficiently. This scenario underscores the pressing need for innovative solutions that enhance the speed and accuracy of handwritten digit recognition. Current methodologies leverage machine learning, particularly deep learning,

which mimics the neural structure of the human brain to improve recognition accuracy as the volume and diversity of training data increase [1]. Despite these advancements, the field still faces significant challenges. These include the inherent variability in handwriting styles influenced by individual differences such as age, gender, and educational background, and technical issues such as ink smudging and variations in paper quality [2], [3], [4]. These factors complicate the recognition process, leading to errors that can have severe implications, especially in sensitive fields like banking where such errors could lead to substantial financial losses.

This study proposes an innovative approach to handwritten digit classification using hardware neural networks and Very-Large-Scale Integration (VLSI). By implementing the perceptron model in a hardware setup and using Verilog as the design language, this research introduces a parallel pipeline tree structure that significantly enhances processing efficiency. The system is designed to handle multiple data streams simultaneously with an array of 256 multipliers and 255 adders, reducing the operational cycle to just 330 clock cycles per digit recognition. This paper details the design and implementation of this system, demonstrating its effectiveness in recognizing handwritten digits from the MNIST database and laying the groundwork for further advancements in machine learning applications for digital text processing.

2. Relevant Applications

2.1 Applications Across Industries

Handwritten number categorization has long been considered a fundamental task in machine learning and computer vision due to its significance across a plenty of industries. Its application makes digital recognition and classification in various industries simpler and more efficient. In the finance and banking industry, handwritten number classification helps automate checks processing. In the postal service and logistics industry, handwritten digit classification can automatically process postal codes or addresses number to reduce labor costs. Moreover, systems can recognize license plate numbers, parking tickets, or boarding passes themselves to improve recording speed and accuracy in the transportation industry [2].

2.2 Current Challenges

Handwritten number classification is widely used in various industries, but it also faces many difficulties and challenges. These challenges come from the diversity of handwritten fonts and the complexity of practical applications. Another type of text is printed numbers, which are easy to classify. Because of the fixed font of printed numbers, the printed digits by machines have more uniform texture patterns, word and letter spacing, and interline spacing [3]. Compared to the printed number, the handwritten number has many uncertain features. Firstly, the handwriting styles of different people vary greatly, making it difficult to have a model to accurately classify all forms of variation. Secondly, the differences in age, gender, and education level among individuals cause significant variations in writing styles. Additionally, some handwritten numbers often overlap or blur, making it difficult to distinguish between two or three different numbers. Finally, the ink fading and smudging of handwritten digits or background noise from printers can increase the difficulty of accurately classifying numbers [4]. The numerical recognition errors caused by these issues will have a significant impact on many industries. For instance, the recognition errors when processing checks are possibly to cause serious financial losses in the bank. Regarding how to solve these difficulties and make improvements, this article conducted research on the classification of handwritten numbers.

3. Project Design

3.1 Hardware Framework

MNIST dataset: This research uses the MNIST dataset as the inputs. The MNIST dataset is a large database containing handwritten digits 0-9. These data are often used for training and testing in image processing and machine learning. The MNIST database contains 60000 training images and 10000 test images. These images were collected by high school students and employees of the U.S. Census Bureau. All the image size format in the MNIST dataset is 28x28 pixels grayscale images. Consequently, the total input contains 784 pixels [5]. Fig. 1 shows an example of 15 sets of 0-9 handwritten digits in MNIST database images.

Fig. 1 An example of 15 sets of 0-9 handwritten digits in MNIST database images (Photo credit: Original).

ISSN 2959-6157

Hardware Neural Network: Hardware neural networks are very helpful and suitable for handwritten numbers classification [6]. Hardware neural networks use models to learn and train the similarity of samples, and after optimization, predict the classification of handwritten digits. It referenced the structure of neurons in the human brain to design the model. Due to the limited computing power of human brain neurons, most models use the most idealized nervous system. Its input layer receives features from the outside, and each input has a strength or weight. This is similar to the synaptic efficiency in biological neurons. Each neuron has a single threshold value. The neuron is activated when the weighted sum of its inputs is produced, and the threshold is subtracted [7]. The neuron's output is generated after the activation signal has been processed by an activation function [6 19-20 page]. This research uses the most well-known and effective neural network model, known as the "perceptron." The model was invented by Frank Rosenblatt, who is the pioneer of the discipline of "Deep Learning." The Fig. 2 shows the structure of the model "perceptron." It applies a nonlinear function to a weighted sum of all of its inputs. The nonlinear function is $\left(\frac{1}{1+e^{-x}}\right)$.

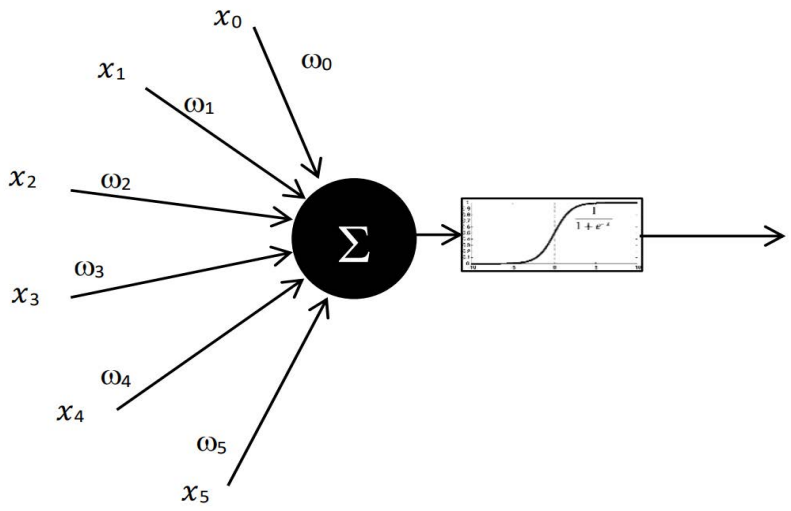

Fig. 2 The model "perceptron" (Photo credit: Original).

Fig. 3 below intuitively describes the architecture configuration of the network. Due to the fact that the images in the MNIST dataset are all 28x28 pixels, there are a total of 784 pixels in the input. Additionally, these are all grayscale images, so it only needs a two-dimensional recognition [8]. Every pixel represents a grayscale image with an intensity value between 0 and 255. For the output shown, there are 10 neurons represent 0-9. Those outputs of the neuron represent the probability of each number from 0-9. All 10 outputs scale from 0-1, and the biggest output is the greatest possibility. The max selector collects and compares the 10 probabilities and output the final possible number. The outputs of the neurons following weight multiplication, summation, and sigmoid, for instance, could resemble this: [Out0 Out1 Out2 Out3 Out4 Out5 Out6 Out7 Out8 Out9] = [0.2, 0.01, 0.006, 0.048, 0.85, 0.063, 0.105, 0.005, 0.0078, 0.09]. The biggest possible is 0.85 which is the fifth number from 0-9. After identifying all of the neural probabilities, the Max Selector block generates a three-bit binary value that represents the highest probability, 3b'100 = 1d'4. This means that the number classification output is a "4" at this time [9].

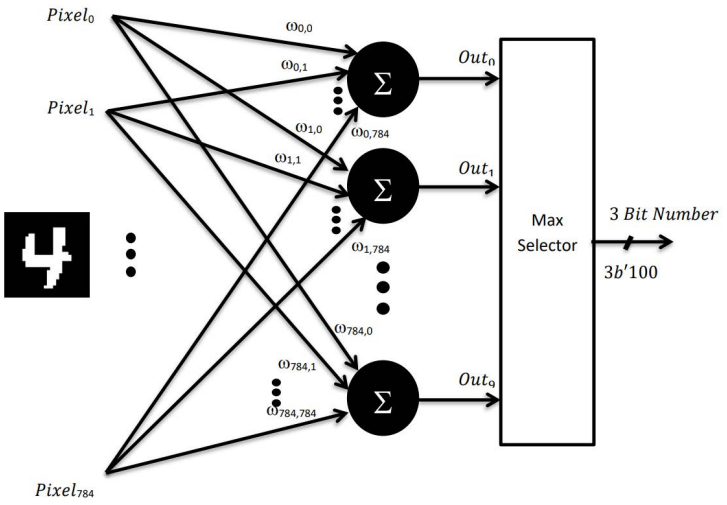

Fig. 3 The architecture configuration (Photo credit: Original).

3.2 System Design

This research utilizes the hardware language Verilog. Verilog is the infrastructure in hardware design, as it supports the development, validation, synthesis, and testing of hardware design. It can effectively describe and validate complex hardware designs [10].

In terms of detailed circuit implementation, Fig. 4 shows the logical flowchart of the hardware design. The 784 inputs represent 784 pixels from the handwritten number pictures. All inputs enter Mux1, Multiplier block, adder block and Mux2 in sequence, and finally give one output which is the most possible number.

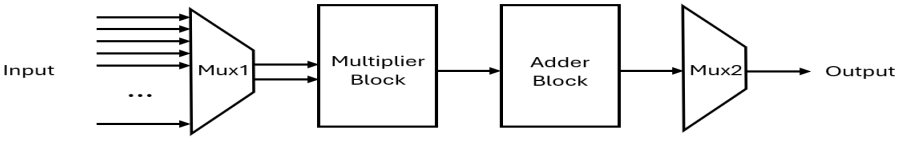

Fig. 4 The logical flowchart (Photo credit: Original).

Mux1: The first Mux is shown in Fig. 5. Originally, there are 784 inputs. This research uses 784+10 inputs, with the addition of 10 Wgt inputs. The 10 Wgt inputs represent the input of 784x10 weight. After selecting appropriate pixels and weights, Mux 1 outputs 256 pixels and 258 weights at every turn.

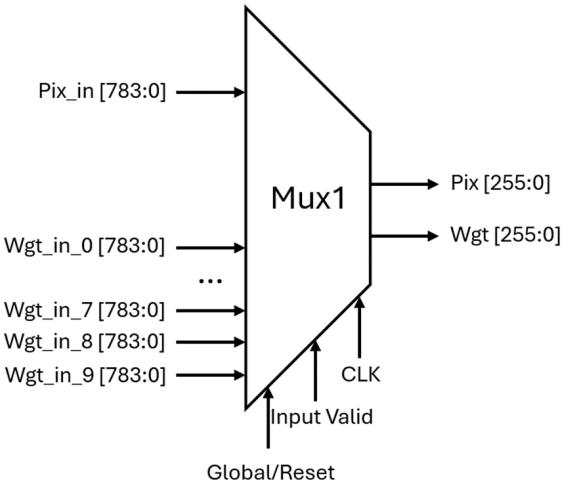

Fig. 5 The first Mux (Photo credit: Original).

Mux2: The second mux is the max selector. Mux2 inputs data processed by multipliers and adders, compares their values, retains the maximum probability as 1, and outputs

ISSN 2959-6157

the corresponding number. As show in the Fig. 6.

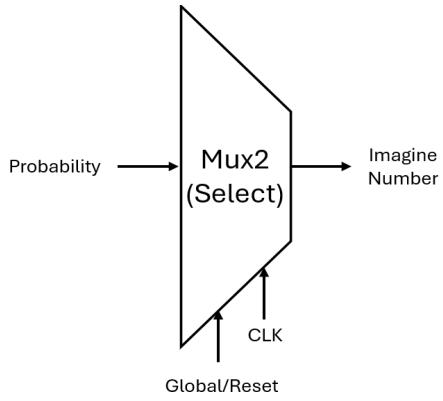

Fig. 6 The corresponding number (Photo credit: Original).

Multipliers and Adders: The Multiplier block contains 256 multipliers, which happens to be 2 to the power of eight. The adder block uses pipelined parallel tree structure which contains 255 adders. The first round had 128 addition operations, followed by 64, 32, and finally only one adder left. This parallel processing pipeline structure effectively reduces the addition operation required for each step by half. This achieves parallel processing and greatly improves computing speed. The reduced usage of multipliers and adders greatly improves operational efficiency. Finally, the accumulator is a register and is responsible for storing intermediate results generated by calculations. Accumulator does not need to write the results back to memory and read them back after each calculation including addition, multiplication, shift, etc. This greatly accelerates the reading speed. As show in the Fig. 7.

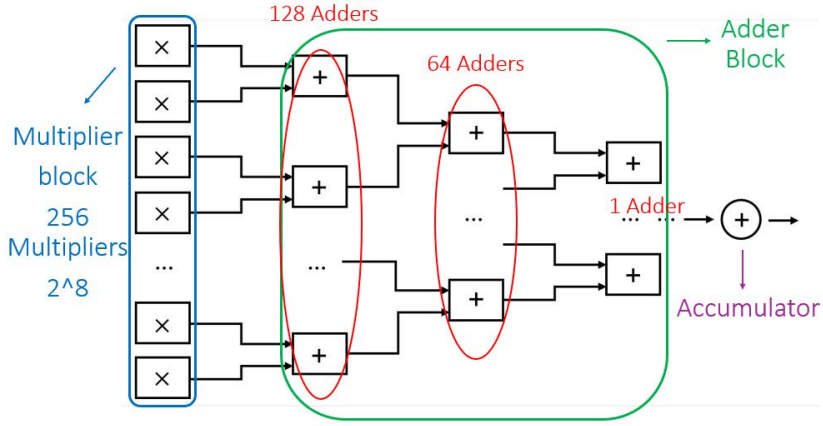

Fig. 7 Parallel Pipeline Structure for Handwritten Digit Classification (Photo credit: Original).

3.3 Performance Evaluation

The testing results are shown in Fig.8 and Fig. 9. The handwritten number classification recognizes and converts the 10 provided handwritten number pictures inputs into binary digits. All tests passed and gave 100 percent successful rate. The delay for each number recognition needs 330 clks.

```
Estimated Output Number is : 0100
Correct Output!! The Classifier has sucessfully classified this image -- PASSED
------------------------------------------------------------
--------------Starting to Test Image Number 8-------------
Actual Number is : 1001
                330 clks of processing done
Estimated Output Number is : 1001
Correct Output!! The Classifier has sucessfully classified this image -- PASSED
--------------Starting to Test Image Number 9-------------
Actual Number is : 0101
                330 clks of processing done
Estimated Output Number is : 0101
Correct Output!! The Classifier has sucessfully classified this image -- PASSED
------------------------------------------------------------
--------------Starting to Test Image Number 10-------------
Actual Number is : 1001
                330 clks of processing done
Estimated Output Number is : 1001
Correct Output!! The Classifier has sucessfully classified this image -- PASSED
------------------------------------------------------------
------------------------------------------------------------
------------------------------------------------------------
---------------------- Total Success Rate =         100 Percent
------------------------------------------------------------
```

Fig. 8 Results of Handwritten Digit Classification Process (Photo credit: Original).

Input	Output	Result	Timing
	0000	Passed	330 clks
	0001	Passed	330 clks
	0010	Passed	330 clks
	0001	Passed	330 clks
	0100	Passed	330 clks
	0111	Passed	330 clks
	0100	Passed	330 clks
	1001	Passed	330 clks
	0101	Passed	330 clks
	1001	Passed	330 clks

Fig. 9 Sample Handwritten Digits from 0 to 9 (Photo credit: Original).

There are 2 main problems encountered during the design. The first one is failed to use two-dimensional array as a module port in Verilog language. It is necessary to convert 28x28 pixels into a vector of 1 times 784 and input it into the neural network. Flatten the 2D array into a 1D vector helps each number in the vector be received one by one by 784 neurons in the input layer. Moreover, implicit port connection is not supported in Verilog. Switch the implicit connections to explicit port connection is important in Verilog (.clk and .clk(clk)).

3.4 Enhancements

For optimization, applying pipelining and optimizing dataflow are essential methods for increasing hardware efficiency. Pipelining reduces total footprint and improves resource consumption by allowing hardware blocks to be reused. It also reduces idle time, which boosts energy efficiency by improving data throughput and lowering power usage. Important strategies include the reuse of processing units, which progressively feed inputs to the same hardware rather than employing different units, and layer-wise pipelining, which processes inputs at each tier of a network simultaneously. These optimizations, for instance, allow for the effective handling of tasks by fewer processing units in FPGA architecture, which reduces both size and energy usage.

4. Advancements in Technology

This study utilizes the perceptron model in hardware neural networks to solve the complex problem of handwritten digit classification. Based on the basic principles of handwritten digit classification, the parallel pipeline tree structure proposed in this study provides a new approach and lays a solid foundation for efficient recognition. The innovative technology of this study significantly reduces the resource utilization of adders and multipliers, greatly improving computation speed and efficiency. The 100 percent pass rate of the experimental results also proves the feasibility of this method. The improvement of handwritten numbers recognition efficiency will greatly benefit various industries. In the current situation of economic growth and increasing material and spiritual needs of people, the workload of many industries is also increasing day by day. In the banking industry, the increase in transactions has led to an exponential growth in the number of checks that need to be processed. The increasing willingness of people to shop online has also led to the need for the express delivery industry to handle more and more package pick-up and delivery. Although there is a handwritten digit classifier, processing a large amount of bank checks and address postal code information can also take too long. It is significant to improve the efficiency of handwritten number classification. The pipeline and parallel processing methods used in this research have enormous potential.

5. Conclusion

This study proposes a more efficient solution and practice for the challenge of handwritten digit classification based on hardware neural networks. Handwritten digit classification technology has a wide range of applications in various industries, such as banking and express delivery industries. At the same time, there are many problems and challenges in the application of handwritten numbers classification. The characteristics of handwritten numbers are highly variable and uncertain. Individual differences among people can lead to significant variations in writing styles. The overlapping or blur of ink and the background noise of the printer can also make handwritten numbers more versatile. The identification errors caused by these factors can cause huge losses to various industries. Consequently, the improvement and innovation of handwritten numbers classification are very important. This research used the MNIST dataset as input and designed circuits using Verilog hardware language. Based on the hardware neural network structure of the perceptron model and the basic principles of model training, this study innovatively

ISSN 2959-6157

uses a parallel pipeline tree structure to connect the multiplier and adder. This method makes resource utilization more efficient, thus greatly improving computing speed. The results presented in practice demonstrate the feasibility of the design, as all ten handwritten number images passed and were correctly classified. Furthermore, the recognition of each number only requires 330 clks, which proves the high efficiency of system. The innovative design of this study provides new ideas for efficient handwritten digit recognition, and parallel pipeline design has great potential in the future. In future design, researchers will attempt to test more images from the MNIST dataset, maintain efficiency while learning and training more diverse handwritten numbers.

In conclusion, handwritten digit classification and recognition remains a complex challenge worth exploring in depth. With the development and improvement of technology, innovation will benefit various industries.

References

[1] A. Nikitha, J. Geetha, D. S. JayaLakshmi, „Handwritten Text Recognition using Deep Learning," 2020 International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT), Bangalore, India, 2020, pp. 388-392, doi: 10.1109/RTEICT49044.2020.9315679.

[2] M. B. Abdulrazzaq, J. N. Saeed, „A Comparison of Three Classification Algorithms for Handwritten Digit Recognition," 2019 International Conference on Advanced Science and Engineering (ICOASE), Zakho - Duhok, Iraq, 2019, pp. 58-63, doi: 10.1109/ICOASE.2019.8723702.

[3] Y. Zhang, H. Xu, X. Zhu, et al., „Detection and Quantization Technique of Optical Distributed Acoustic Coupling Based on φ-OTDR," J. Shanghai Jiaotong Univ. (Sci.), vol. 25, pp. 208-213, 2020.

[4] S. Das, „Hand-Written and Machine-Printed Text Classification in Architecture, Engineering & Construction Documents," 2018 16th International Conference on Frontiers in Handwriting Recognition (ICFHR), Niagara Falls, NY, USA, 2018, pp. 546-551, doi: 10.1109/ICFHR-2018.2018.00101.

[5] O. Surinta, M. F. Karaaba, L. R. Schomaker, M. A. Wiering, „Recognition of handwritten characters using local gradient feature descriptors," Engineering Applications of Artificial Intelligence, vol. 45, pp. 405-414, 2015, https://doi.org/10.1016/j.engappai.2015.07.017.

[6] R. K. Mohapatra, B. Majhi, S. K. Jena, „Classification performance analysis of MNIST Dataset utilizing a Multi-resolution Technique," 2015 International Conference on Computing, Communication and Security (ICCCS), Pointe aux Piments, Mauritius, 2015, pp. 1-5, doi: 10.1109/CCCS.2015.7374136.

[7] H. Xu, X. Zhu, Z. Zhao, X. Wei, X. Wang, J. Zuo, „Research of Pipeline Leak Detection Technology and Application Prospect of Petrochemical Wharf," 2020 IEEE 9th Joint International Information Technology and Artificial Intelligence Conference (ITAIC), Chongqing, China, 2020, pp. 263-271.

[8] X. Liang, V. Dutt, S. Dutt, Y. Luy, „Handwritten character recognition using artificial neural network," Advances in Computing, vol. 1, no. 1, pp. 18-23, 2011, https://doi.org/10.5923/j.ac.20110101.03.

[9] Z. Lin, „Hand-Written Number Classification Based on Hardware Neural Network," 2023 IEEE International Conference on Electrical, Automation and Computer Engineering (ICEACE), Changchun, China, 2023, pp. 1447-1451, doi: 10.1109/ICEACE60673.2023.10442222.

[10] D.Thomas, P., & Moorby, (2008). The Verilog® hardware description language. Springer Science & Business Media.