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Proteus Based Digital Ranking System

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Abstract:

In sport competitions that require hedge line to be ranked, accurate line ranking can effectively improve the fairness and professionalism of the competitions, and it is an indispensable part of the regular game. However, ranking systems on the market are usually of high cost and difficult to operate, which improve the cost of competitions organizers and entry threshold. This hinders carrying out unofficial games in the society. To address this situation, the article will design a digital ranking system based on the Proteus platform, using basic logic gates, counters, selectors, shift registers, decoders and encoders, with the goal of displaying the order in which the targets were passed, and with a reset function. After careful design, the ranking system is able to accurately display the order of the targeted routes and fully reset itself. After simplifying the design, the system has the characteristics of simple construction, low cost and easy to use, to achieve the goal of applying to small unofficial competitions. The article will focus on the methods of using, the working principles, and the areas for improvement of ranking systems.

Keywords: Ranking system; shift registers; dynamic scanning of digital tubes.

1. Introduction

With the popularization of national sports in China [1], the professionalism of the people's sports is rising. Enthusiasts are no longer satisfied with the usual individual practice, and gradually put their eyes on the competition. As a result, there has been a prominent increase in the number of unofficial competitions in various sports in society [2]. Providing accurate results ranking is a very key part of the game in some events such as road cycling, marathon and other events that need to rank the results of the line because accurate ranking can effectively improve the fairness and professionalism of the game [3] and is conducive to the development of the sports cause of the project. However, the professional competition facilities such as the electronic timing system used in these competitions are not only expensive but also troublesome to set up, requiring many people to operate at the same time and professional knowledge of operating skills. Therefore, these professional systems consume a lot of manpower and material resources and are not in line with the low-cost concepts of social and unofficial competition resulting in their difficulty in being used in small-scale competitions in the community. Therefore, the market is currently lacking a convenient to use, can provide accurate ranking system. This system is very meaningful for these small-scale competitions because it can effec-

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tively reduce the cost of these competitions, facilitate the development of competitions, but also reduce the entry threshold of participants.

This paper will be based on the Proteus platform, design a digital ranking system, about its specific use, working principle and to be improved.

The article consists of five chapters, the first chapter is the introduction, the second chapter is the use of the system, explaining the specific use of the system, the third chapter is the system components, explaining the four components of the system and its working principle, the fourth chapter is the shortcomings of the system, analyzing the shortcomings of the system, and giving the ideal solution. The fifth chapter is the summary, which summarizes the content of each chapter of the paper.

2. Organization of the Text

2.1 the specific use of the system

First of all, put a sensor chip on each object that needs to be ranked [4], and put a sensor line on the place that needs to be ranked. When the object passes through the sensor line, it triggers the switch once. The digital tube shows 4 zeros when no object passes through the sensor line, when the first object passes through, the serial number of the sensor line that the object passes through will be displayed on the right side of the digital tube. When a new object passes by, the original serial number of the display moves one bit to the left, and the new serial number appears on the far right. After four serial numbers are triggered, the four positions of the digital tube are occupied. The serial number ranking of the digital tube from left to right is the order in which the objects pass through the sense line. When the ranking is finished, press the reset button of the system to reset the system and all the previous ranking information of the system is cleared, and the digital tube displays four zeros again. The system is ready for a new round of ranking. The following Figure 1 is an overview of the circuit of the ranking system.

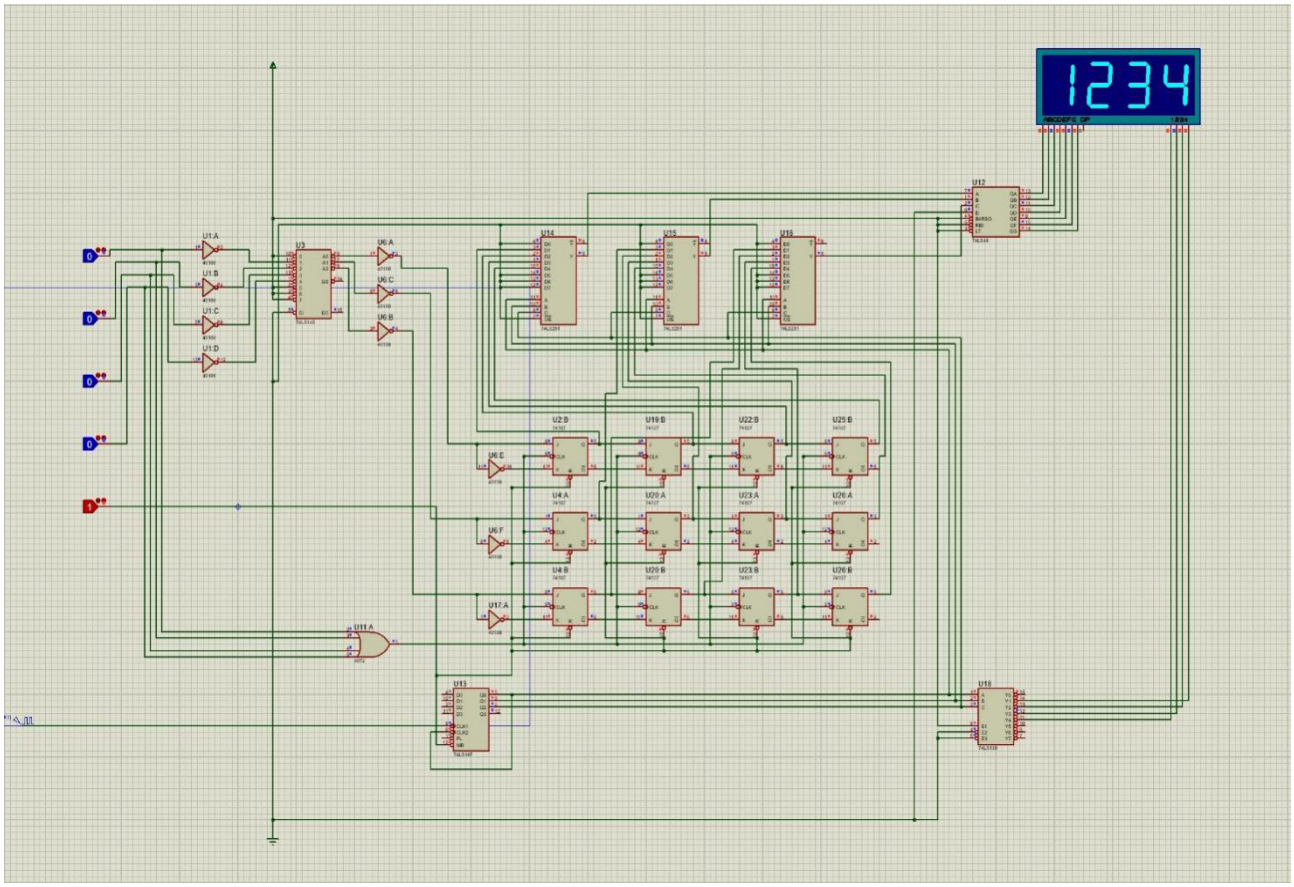

Fig. 1 The overview of the digital ranking system circuit

2.2 System component

The ranking system can be divided into four basic parts, the first part is the signal acquisition part, the second part is the signal data storage part, the third part is the ranking display part, and the fourth part is the reset system. The following article will focus on these four parts

2.2.1 Signal acquisition systems

The signal acquisition system includes signal acquisition switch and encoder. The following Figure 2 shows the circuit overview of the signal acquisition system part.

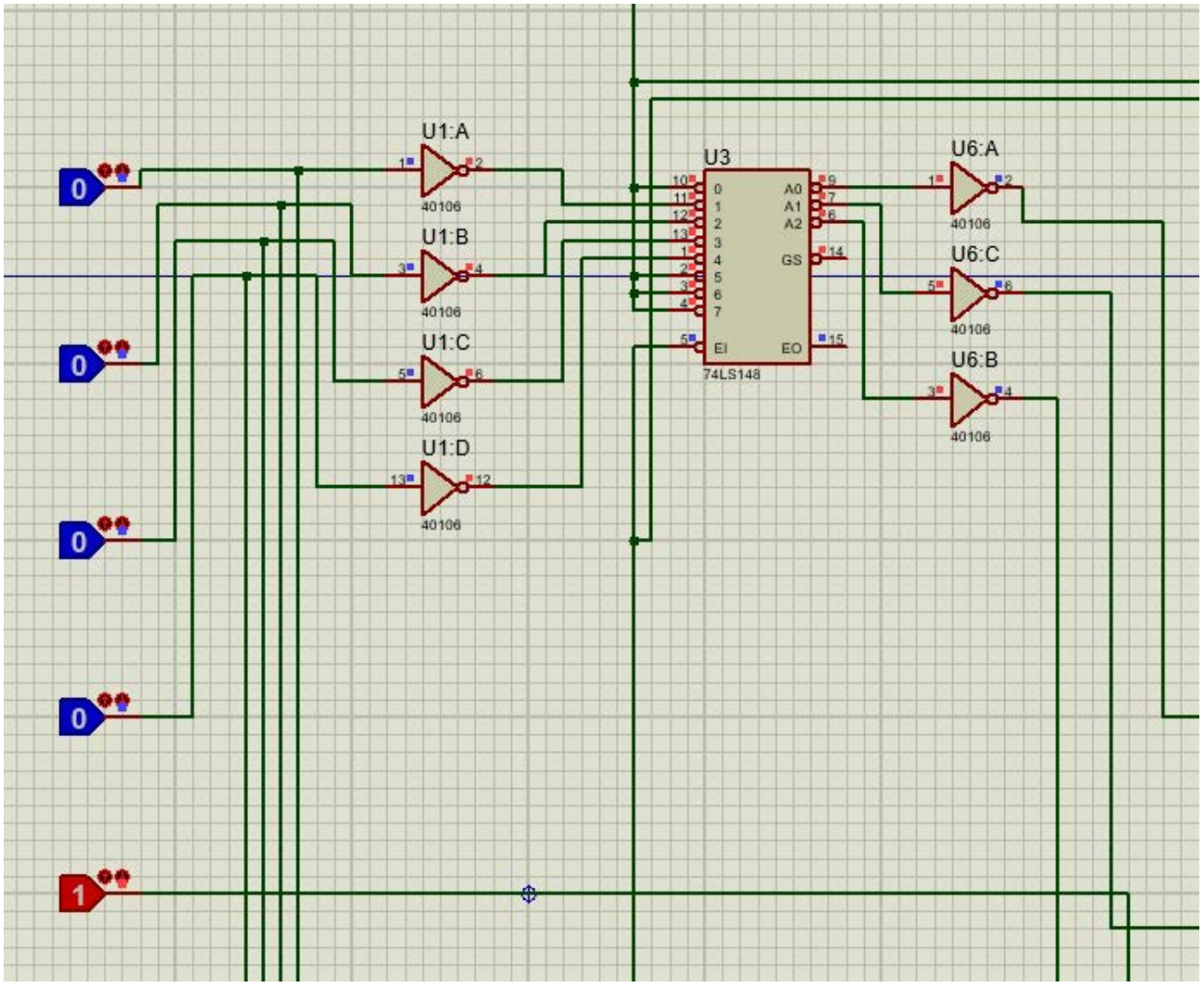

Fig. 2 The overview of the signal collecting system circuit

As shown in Figure 2, the five logical switches on the left are signal acquisition switches, of which the top four are the four trigger signals that will be ranked, and the bottom one is the reset trigger signal. In this design, all five switches must be self-resetting switches, that is switches that can be triggered once to shift the level from 0 to 1 and from 1 to 0[5]. This feature has important function in the following circuit logic design, which will be explained in detail in the following article. Trigger switch triggers once When it detects the signal. Since the encoder 74LS148 used later is a low-level active encoder and the acquired signal is high-level active, an inverter needs to be connected between the logic switch and the encoder respectively to convert the high-level active signal to low level active.

Next connect the 74LS148 which is an 8-input 3-output priority encoder [6], the encoder is responsible for recording the positional information of the trigger signal: bit 1, bit 2, bit 3, bit 4, and converting this four positional information into easy-to-store binary coded information. Likewise, the output binary code is an inverted code, so an inverter is connected to each output bit of the encoder to convert the binary code to the original code. The input end of the encoder is actually only used for bits 1 to 4 because

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there are only four actual trigger signals this time. The rest of the input ports are grounded. EI is the gated input end, and it is low-level active. It is also grounded because it needs to be triggered all the time. The outputs use a total of three ports A0 A1 A2 and the rest of the ports are not required. The following Table 1 shows the truth table of 74LS148.

Table 1. The truth table of 74LS148

EI	0	1	2	3	4	5	6	7	A2	A1	A0
H	*	*	*	*	*	*	*	*	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H
L	*	*	*	*	*	*	*	L	L	L	L
L	*	*	*	*	*	*	L	H	L	L	H
L	*	*	*	*	*	L	H	H	L	H	L
L	*	*	*	*	L	H	H	H	L	H	H
L	*	*	*	L	H	H	H	H	H	L	L
L	*	*	L	H	H	H	H	H	H	L	H
L	*	L	H	H	H	H	H	H	H	H	L
L	L	H	H	H	H	H	H	H	H	H	H

2.2.2 Data storage component

Next comes the second part, the signal data storage part. This part is mainly a register. Below is Figure 3, an overview of the circuit in the data storage section.

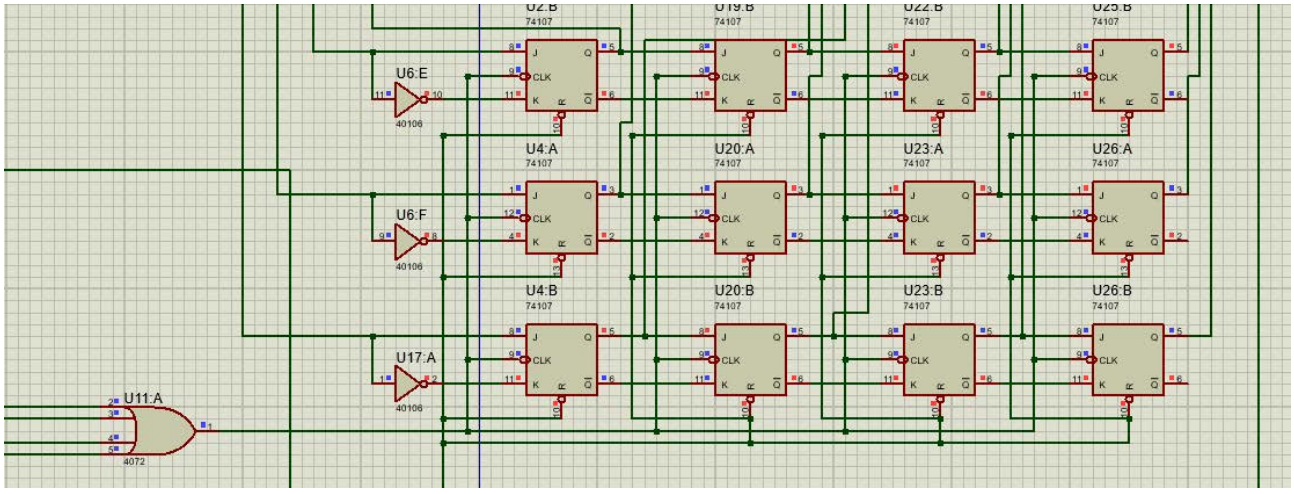

Fig. 3 The overview of the data storing system circuit

Due to the particularity of this part in the storage of data, the author will explain at the same time. As can be seen from the figure, the left side of this part is a four-input or gate, respectively directly connected to the input trigger switch, through the door connected to the clock input of four groups of registers. On the right are four sets of series-connected triple-parallel falling-edge-triggered JK flip-flop[7]. Each group corresponds to a ranked bit, and the triple parallel triggers inside each group correspond to a bit in the binary code. The following Table 2 shows the function table of the falling edge triggered JK flip-flop used.

Table 2. The function table of negative-edge-triggered JK flip-flop

SD'	CD'	CP'	J	K	Q^n	Q^{n+1}	Q^{n+1r}
0	1	x	x	x	x	1	0
1	0	x	x	x	x	0	1
1	1	⬇	0	0	0	0	1
1	1	⬇	0	0	1	1	0
1	1	⬇	0	1	0	0	1
1	1	⬇	0	1	1	0	1
1	1	⬇	1	0	0	1	0
1	1	⬇	1	0	1	1	0
1	1	⬇	1	1	0	1	0
1	1	⬇	1	1	1	0	1

The four-input or gate function on the left is the clock input of the register. When any one of the trigger switches is triggered, the trigger signal will go through the process of 0 to 1 and 1 to 0. During the process of 0 to 1, the clock input will change from low level to high level. While the register receives a set of data, but the data does not move to the next bit due to the fact that the JK flip-flop is triggered along the falling edge. When the trigger signal changes from 1 to 0, the JK flip-flop triggers along the falling edge, and the JK end of the JK flip-flop reads a signal that is still high due to the delay in reading signals from the JK flip-flop [8]. The JK flip-flop transmits the read signal to the next digit according to the truth table. This completes the clock signal of a cycle.

On the right is a serial-input parallel-output register consisting of four sets of series-connected triple-parallel falling-edge-triggered JK flip-flops, with an overall storage specification of 3X4 totaling 12 bits. The system uses JK flip-flops because Proteus does not provide falling-edge-triggered D flip-flops in the component library. Each set of flip-flops consists of three flip-flops in parallel, with the top flip-flop storing A0, the second flip-flop storing A1, and the third flip-flop storing A2. There are four sets of triggers, the first set stores the first trigger signal, the second set stores the second, the third set stores the third, and the fourth set stores the fourth. Four sets of triggers in series. When a clock signal comes, the data currently stored in each group moves to the next group and the new set of data is stored. When only one trigger switch is triggered, the position data is in the first set of triggers and the remaining triggers store empty data. When all four trigger switches are triggered, the first position data is in the fourth set of triggers, the second position data is in the third set of triggers, and so on. All four-position data are stored.

After the above steps, the location data is saved in the register according to the trigger order and the data storage part is completed.

2.2.3 Ranking display component

The third part is the ranking display part. The function of this part is to read the position data in the register and display the data in turn in the digital tube. It is mainly composed of the data selector and the digital tube. The digital tube display adopts a high-frequency dynamic scanning display[9], that is the digital tube displays different numbers in different positions at high frequency, utilizing the afterglow effect of the digital tube to let the numbers stay on the digital tube. The idea of location determines the number is used in the display aspect, that is, the display position of the digital tube is lit up in order, and then the display position determines the specific display content. The following Figure 4 is an overview of the circuit in the ranking display section.

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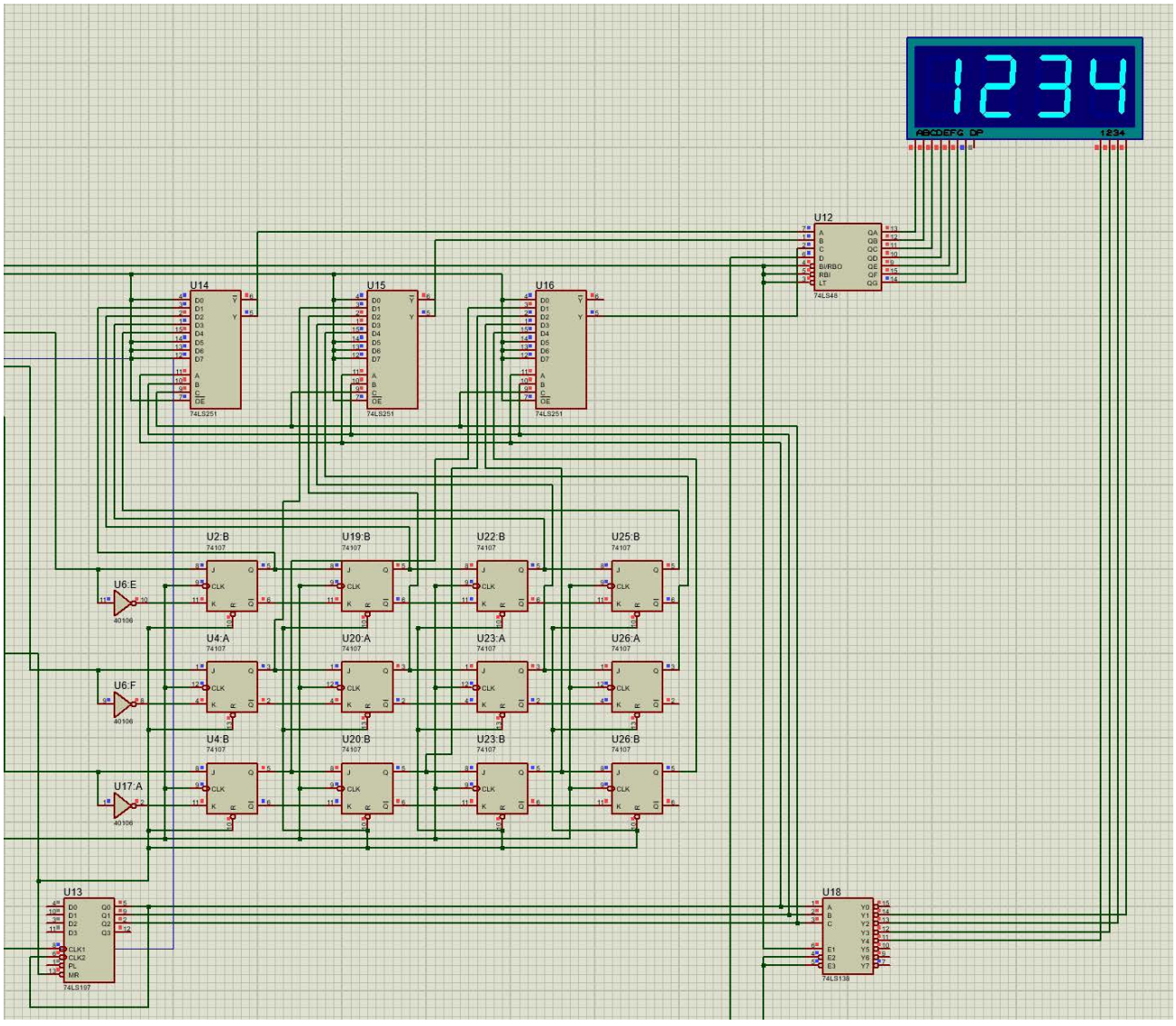

Fig. 4 The overview of the rank displaying system circuit

In the lower left is a 74LS197 that is a hexadecimal counter, the output interface of the counter clock interface access to a clock signal with a frequency of 10kHz. The counter only needs to use the first three output interfaces because there are only four trigger signals need to be sequence. First, connect the 74LS138 which is a 3 input 8 output decode. The output of the decoder is low-active. When the counter enters a binary code, the output port at the corresponding position of the decoder changes to 0. When the counter enters 1, the Y1 position of the decoder takes effect. The data on the leftmost side of the register lights up on the rightmost side of the digital tube. The position where the decoder Y1 is connected to the digital tube takes effect on the rightmost side of the input port. When the counter input 2, the Y2 position of the decoder takes effect and the data of the left two of the register is illuminated in the right two of the digital tube. The decoder Y1 is connected to the digital tube to take effect the right two of the input port. And so on.

Above the register are three 74LS251, an eight input data selectors [10], each of which corresponds to one bit of the binary code of the number to be displayed. The leftmost selector corresponds to the a0 bit, the middle selector corresponds to the a1 bit, and the rightmost selector corresponds to the a2 bit. The selection input port ABC of the three groups selector inputs the position of the data to be output. When the counter inputs 1, the digital tube displays the data on the leftmost side of the register, at this time ABC should be 001. When inputs 2, the digital tube displays the data on the left second of the register, at this time ABC should be 010. And so on. The first group selector D1~D4 respectively access the a0 bit of four groups of registers, the second group selector D1~D4 respectively access the a1 bit of four groups of registers, the

third group selector D1~D4 respectively access the a2 bit of four groups of registers. When no departure switch has been triggered, the counter outputs 0 and the selector ABC code inputs 000, at which time no register data is selected, so the digital tube displays 0.

Each of the three sets of registers is connected to a 74LS48, a seven-segment display decoder[11], and the input port is ABCD, which corresponds to bits a0~a3 of the input binary code. The digital tube displays the actual number corresponding to the binary code. Since the numbers displayed are only 0 to 4, only three inputs ABC are needed. A connects to the first set of registers, B connects to the second set of registers and C connects to the third set of registers. Output ports QA~QG are connected to the content display input ports A~G of the digital tube respectively. The following Figure 5 shows the output relationship of the 74LS48 corresponding to the seven-segment digital tube.

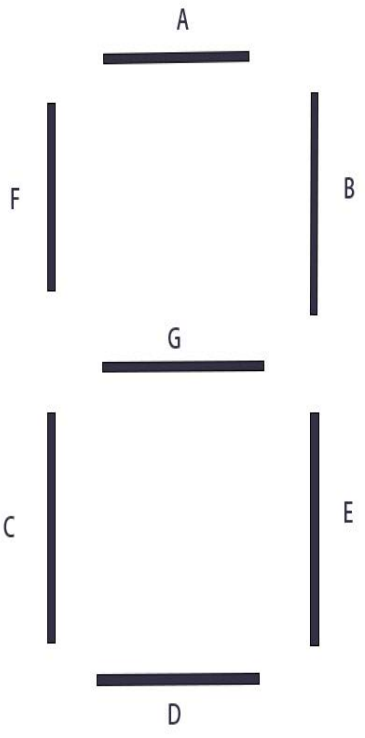

Fig. 5 The mode of digital displaying

Since then, when the counter outputs X, the digital tube selects the contents of the X register to output in the X position from the right. When the clock frequency is high enough, all 4 digits can be displayed by the digital tube at the same time. When the trigger switches are pressed one by one, the digital tube will display the serial numbers of the switches from right to left according to the order in which the switches are pressed. The ranking completes.

2.2.4 System reset component

At the bottom of the five trigger switches on the far left of the system is a self-reset switch, low- active. The switch is followed by the reset input of all integrated logic in the system. When the reset input completes one cycle, all data in the integrated logic will be forcibly cleared to complete the reset of the system. The reset system operates at a high level. When the ranking is finished and a new round of ranking is needed, it needs to be pressed once to complete the reset of the system and prepare for the next round of ranking.

This is how the ranking system is implemented.

2.3 Discussion

Some of the shortcomings of this system are described below.

2.3.1 No overlapping of signals

Since the clock signal driving the register feed is implemented by an or gate, the clock signal remains high when two or more trigger switches are turned on at the same time. When the last trigger signal switches from 0 to 1, the clock signal will enter the falling edge. At this time, the register will be driven and at this time, the register can only store the last trigger signal, while ignoring the same time and the earlier end of the rest of the trigger signal, resulting in the digital tube only showing a trigger signal. As shown in the figure below, when the trigger switch 1 and 2 are triggered at the same time and the switch signal 2 ends later, the digital tube will only display switch 2 and ignore switch 1. The following Figure 6, Figure 7 and Figure 8 show the process when switch No. 1 and switch No. 2 are triggered at the same time, the signal No. 2 ends later, and the ranking system will only show No. 2.

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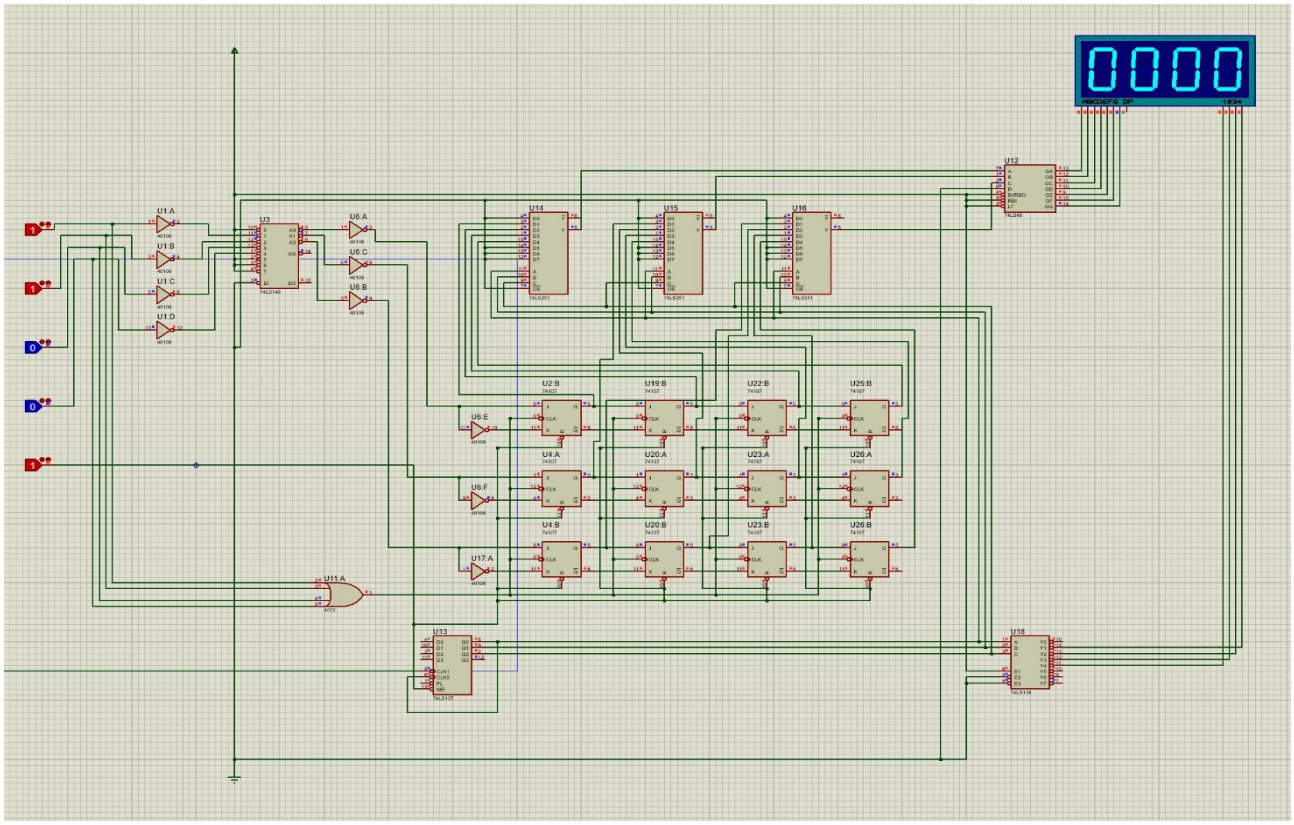

Fig. 6 The overview of the circuit when switch 1 and switch 2 are triggered

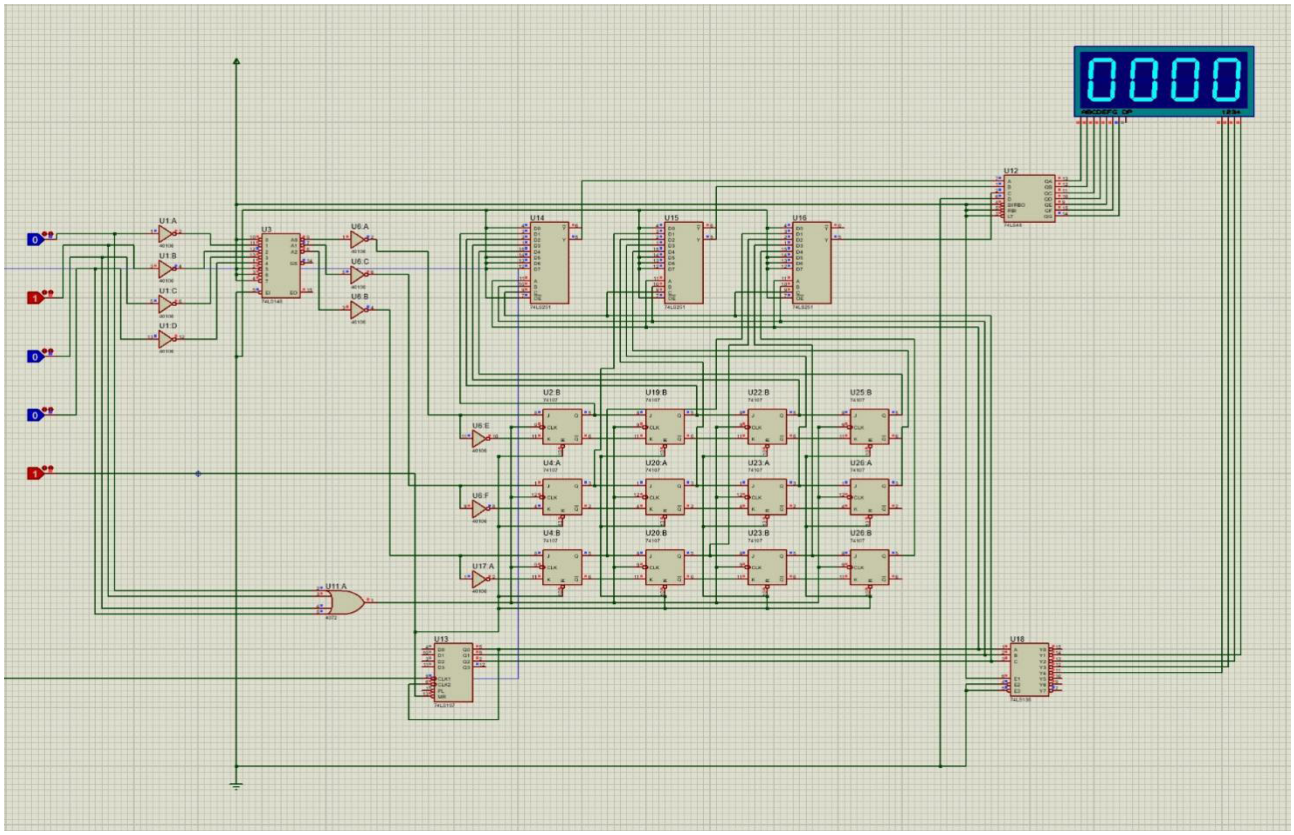

Fig. 7 The overview of the circuit when signal 1 is finished while signal 2 is unfinished

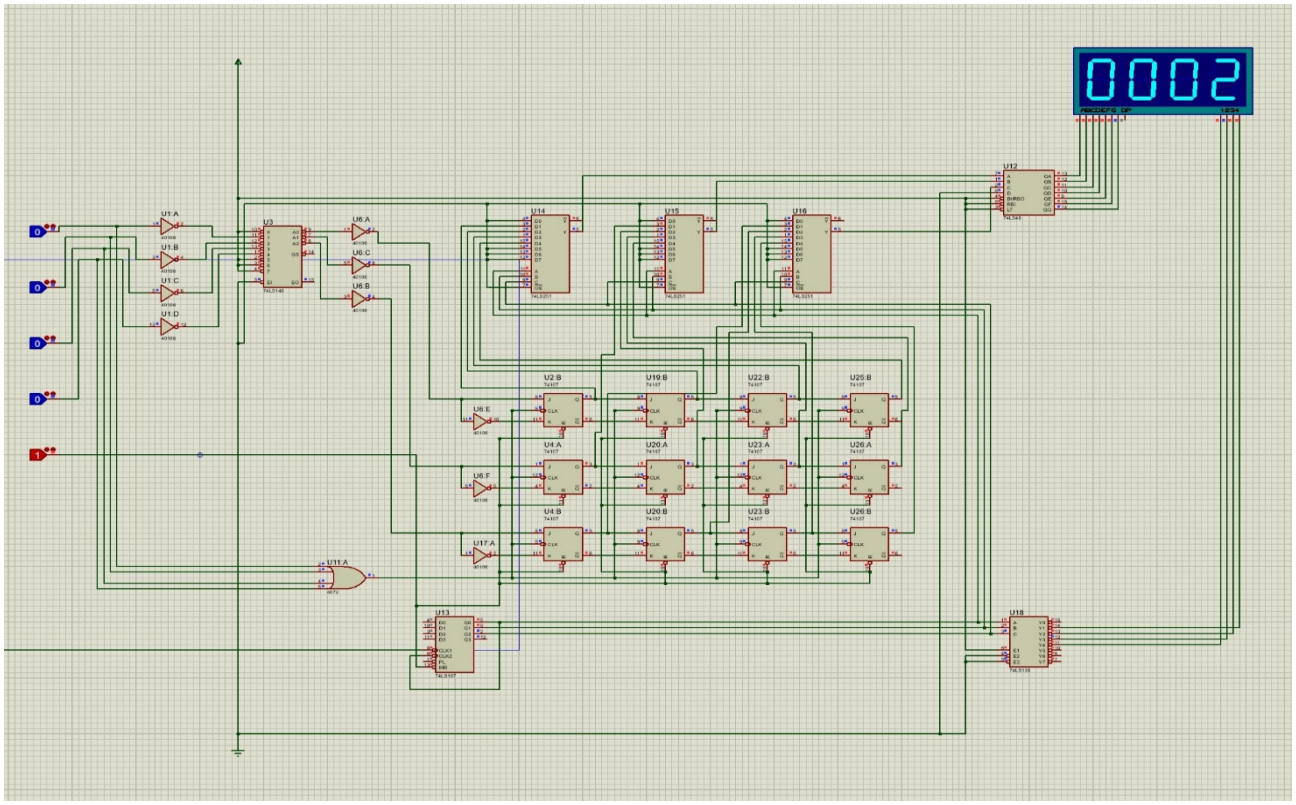

Fig. 8 The overview of the circuit when signal 2 is finished after signal 1

The solution to this problem is to use a self-resetting switch with the shortest possible trigger signal period to reduce the probability of trigger signal overlap. Ideally, the trigger signal becomes an impulse signal. There is always a small time difference between trigger time in the actual use of the trigger signal in the strict sense, so there will not be any overlapping, thus solving the problem. But in practice, the trigger signal cannot be an impulse signal. As a result, as far as possible to reduce the period of the trigger signal is the key to ensuring the normal operation of the system and improving the accuracy of the measurement.

3. Summary

This paper describes a digital ranking system based on Proteus design. In the part of the system use method, it is necessary to prepare the induction chip and the induction line. When detecting the object carrying the induction chip through the induction line, the system can rank the order of the object going through the induction line. In the system composition part, the ranking system is divided into four main parts. First of all, the signal acquisition system collects the trigger signal and converts it into binary code respectively. The binary code enters the data storage part, and is stored into the four groups of JK triggers in sequence respectively. Finally, the data in the register is read at high frequency through the selector which has accessed the high-frequency clock signal. By using the method of position-determined digit, it scans dynamically to let the The digital tube displays the trigger sequence of the trigger signal. When a new round of ranking is to be carried out, the reset switch is used to input a clear signal to all integrated logic in the system and clear all data in the system to achieve the effect of setting. The discussion part describes the shortcomings of the system, that is, the triggering process of the trigger signal cannot overlap, which can be solved by using the trigger switch with the trigger signal period as short as possible. The ranking system has been designed with simplified logic to achieve the goals of simple construction, low cost and ease of use. It is an ideal ranking system for use in unofficial social competitions.

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