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Research on Key Technologies for Chip Area and Power Optimization in Low-Powered Digital Integrated Circuit

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Abstract:

With mobile technology being the norm and the need for more computational power for applications such as AI, simulations and virtual reality, integrated circuit chips are required to be smaller to be more power efficient at the same time be more powerful than its predecessors. This paper aims to discuss and present the techniques and technologies involved in optimizing the power consumption and chip area of low-powered digital integrated circuits. In this paper, the CMOS integrated circuit would be the main focus for discussion. The main discussions would be on the subject of various techniques to improve power efficiency and reduce chip area in a low powered CMOS integrated circuit. The two sources of power consumption and factors that affect it would be identified and solutions to reduce power consumption based on each factor would be brought up. Circuit area optimisation would also be discussed at both the design and manufacture level.

Keywords: CMOS integrated circuit, low power, chip area optimisation.

1. Introduction

Integrated circuits since its introduction in the 20th century has become a staple in modern commercial electronics. In 1958, the first integrated circuit is brought into the light by Jack Kilby made using a slice of germanium as a bulk resistor and integrating a single bipolar transistor [1]. Eventually, integrated circuits became more complex containing more and more components to meet desired performance and functionalities. The Intel 4004, the first commercially available microprocessor launched in 1971 contained 2300 transistors. By 2010, an Intel Core processor contained around 560 million transistors. This exponential increase in transistor density corresponds to Moore's Law which predicted that the number of transistors in a chip would double every two years [2]. This prediction has since been highly debated and some claim it no longer holds true, but one thing's for sure, the number of transistors in a chip in the future would be much larger than current chips.

This situation give rise to two issues that needed to be resolved: the power consumption of circuits getting higher with more components and the surface area of the chip increasing. Higher power consumption would cause higher heat output and would

require robust power supply units. This could be said the same for larger chip area. Finding adequate heating solutions would become very difficult. In addition to that, it would make mobile devices to be impossible as integrated circuits with high power consumption requires the use of a large battery and large integrated circuits would use up a lot of space.

The discussion begins in Section 2 with power optimisation of integrated circuits. Within section 2, section 2.1 discusses the source of power consumption in a CMOS circuit. Later in section 2.2, the various methods to reduce power consumption based on each source mentioned in section 2.1 are laid out. In section 3 the subject of chip area optimization is dissected and techniques on improving chip area and transistor density. Lastly, section 4 act as the summary of this paper.

2. Power optimisation in a CMOS Integrated Circuit

2.1 Source of Power Consumption in a CMOS Circuit

In a traditional CMOS circuit, multiple PMOS and NMOS transistors are connected together with a minimum of one NMOS transistor being connected to a PMOS transistor at both of their respective drains. The connected drain acts as the output and the gates are used as inputs. Figure 1 shows a simple inverter made using CMOS. At steady state, CMOS has a power consumption that is negligible. Hence, it is a great candidate for low powered integrated circuits.

Fig.1 A simple CMOS inverter

There are two main source of power consumption in CMOS circuits, dynamic power and static power. Dynamic power is the power consumed by the CMOS circuit when bits are switched from '0's to '1's in vice versa. Static power is power consumed when the circuit is in steady state, normally due to leakage current. In circuits with large CMOS feature size, static power is much smaller compared to dynamic power. However, as CMOS feature size become smaller especially CMOS integrated circuits with gate length of under 90nm [3], the static power becomes significant and must be taken in account.

Dynamic power manifests primarily in the form of capacitive power. Capacitive power is cause by switching between different states, i.e. between '0's and '1'. The amount of power consumed by the switch could be calculated using the following formula:

$$P_{capacitive} = \alpha C_L V_{DD}^2 f \tag{1}$$

where α = Activity factor, C_L = Load Capacitance, V_{DD} = Supply voltage, f = Clock frequency

This power consumption is caused by the fact that the load capacitance of the NMOS and PMOS transistors in a CMOS circuit needs to be charged and discharged when switching states. With the activity factor and the load capacitance of the CMOS circuit to constant, it leaves the supply voltage and the clock frequency to be the main contributing factor of power consumption in a CMOS circuit.

Alongside capacitive power, short-circuit power is also dissipated when switching states. There is a brief moment where both NMOS and PMOS transistors are conducting at the same time while switching which would 'short' the supply voltage to ground. The short circuit power could be assumed to be:

$$P_{short-circuit} = I_{sc} \cdot V_{DD} \cdot f \tag{2}$$

where I_{sc} = Short-circuit current during switching, V_{DD} = Supply voltage, f = Clock frequency

Generally, short-circuit power is regarded as a smaller contributor in the face of capacitance power. Nevertheless, it is also mainly affected by supply voltage and clock frequency which means it has significance at higher supply voltages and at high frequencies.

The second category of power consumption in CMOS integrated circuits is static power consumption in the form of subthreshold leakage power. Subthreshold leakage occurs when the transistor is not active. Due to small subthreshold voltage being present across the transistor, a small current flows between from the drain to source. The subthreshold leakage current could be expressed with the following equation [4]:

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{-\frac{V_{ds}}{V_T}}\right] \tag{3}$$

$$I_0 = \frac{W \mu_0 C_{ox} V_T^2 e^{1.8}}{L} \tag{4}$$

where V_T = Thermal Voltage, V_{th} = Threshold Voltage, V_{ds} = Drain Source Voltage, V_{gs} = Gate Source Voltage, C_{ox} =

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Gate Oxide capacitance, μ_0 = Carrier Mobility, n = Sub-threshold Swing Coefficient

As CMOS feature size shrinks, static power consumption becomes a challenge in the process of reducing power consumption of integrated circuits.

The total power consumption of a CMOS circuit is the sum of both dynamic and static power consumption and could be simplified as:

$$P_{total} = P_{capacitive} + P_{short-circuit} + P_{leakage} \quad (5)$$

2.2 Methods to lower power consumption in a CMOS circuit

Based on the equations in the previous section, the main contributing factors of power consumption are the supply voltage, V_{DD}, load capacitance, C_L, activity factor, α and clock frequency, f.

By lowering the supply voltage, both the capacitive power and the short-circuit power would be lowered. However, there are a few things to take note of. A low supply voltage could lead to decreased performance of the circuit as it would introduce delays. The relationship between delays in a transistor and supply voltage is as follows:

$$t_{delay} \propto \frac{V_{DD}}{(V_{DD} - V_{th})^2} \quad (6)$$

where V_{DD} = Supply Voltage, V_{th} = Threshold Voltage

According to this relationship, as the supply voltage decreases the delay of the transistor would increase. In order to mitigate the effects of low performance due to low supply voltage, adaptive voltage scaling (AVS) could be implemented. This technique dynamically adjusts the supply voltage depending on the workload and required performance, allowing overall lower power consumption. One of the approaches for AVS is the critical path emulator [5]. Through emulation, the critical path delay at a given condition and target speed of the chip could be predicted. The supply voltage is then adjusted such that the minimum power required for the target task is supplied.

The clock frequency is also the main contributing factor of power consumption in a CMOS integrated circuit as it would affect the rate at which switching occurs. Low clock frequency just like low supply voltage would cause a reduction in performance of the CMOS circuit. In order to reduce power consumption without sacrificing performance, a few approaches are used. One of the methods is asynchronous circuit design where the global clock is removed and circuits are split into multiple subcircuits. Each subcircuit could have its own local clock and communicate with each other using handshake protocols, through request and acknowledgement signals. This approach allows subcircuits to remain at standby mode until needed, reducing the power consumption of the system [6].

Another way to reduce the effect of frequency on power consumption is through clock gating. When a certain part of the circuit is not in used, the clock signal to that portion of the signal would then be disabled to reduce unnecessary switching activities [7]. Figure 2 shows a basic latch-and gate based integrated clock gating cell (ICG).

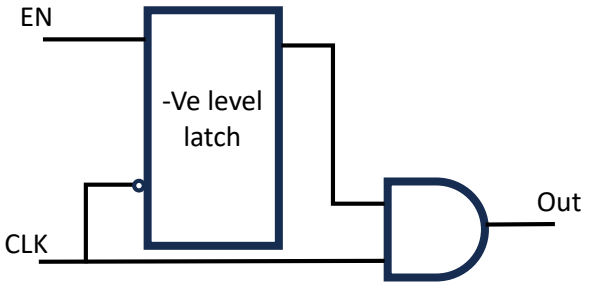

Fig.2 Basic latch-and gate based integrated clock gating cell (ICG)

EN is the clock enable signal input and CLK is the main clock signal. When the clock enable input signal is high, the clock signal would be connected to the output. A latch is added in front of the AND gate to prevent glitches during transition of enable clock signal.

Power consumption could also be reduced by reducing the capacitance of the CMOS circuit. There are two main sources of capacitance in a circuit, capacitance caused by the transistor and capacitance caused by wiring [8]. Using low-k (low dielectric constant) materials between metal layer and substrate of the transistor could reduce its capacitance. By decreasing the length of the wires between transistors in the CMOS circuit the parasitic capacitance could be decreased. Increasing clearance between the wires could also decrease the capacitance.

Finally, the reduction in activity factor of the circuit could also reduce the power consumption of the CMOS circuit. By optimising the logic and reducing the number of transistors, the activity factor could be reduced significantly which in turn, translates into reduction in power consumption. On a side note, a technique mentioned previously, clock gating could also potentially reduce activity factor by making subcircuits that are not in use inactive.

3. Chip Area Optimisation of a CMOS circuit

Techniques to minimise the chip area of a CMOS circuit could largely be categorised into two categories, logic level or circuit level optimisation, manufacturing and transistor sizing. Logic level optimisation reduces the number of redundant components within a circuit while advance

transistor manufacturing allows the reduction in size of transistors which would take up lesser space.

On the circuit level, the identification and elimination of redundant components could be done by analysis of the circuit. As an example, figure 3 shows a XOR gate with one inverted input in the logic gate layout and the transistor layout.

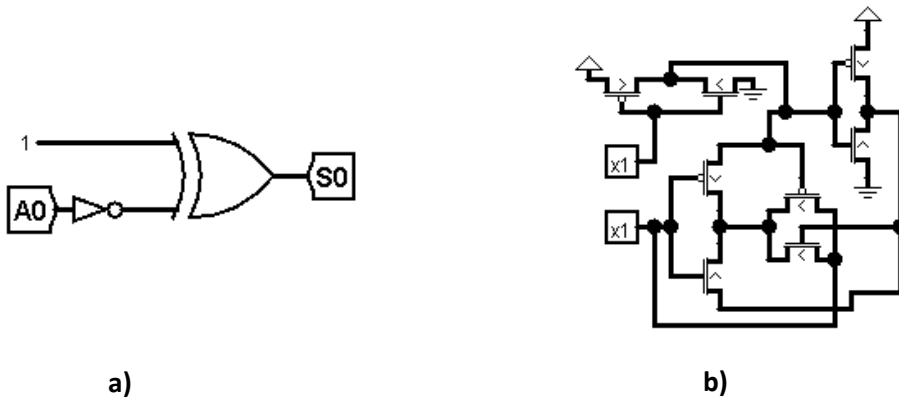

Fig.3 A XOR gate with one inverted input in (a) the logic gate layout and (b) the transistor layout

The transistor layout is a unoptimized conversion of the logic gate layout. Upon close inspection, one of the inputs is inverted twice when only one inversion is needed. Hence, by rerouting the circuit, one inverter could be removed. Figure 4 shows the optimised transistor circuit.

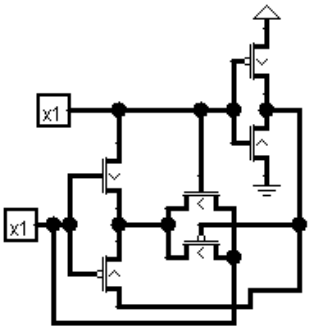

Fig.4 The optimised transistor circuit

The number of transistors of the circuit is reduced by 25% from 8 transistors to 6 transistors. If a CMOS circuit uses multiple of the above mentioned subcircuit, it would bring about a great decrease in chip area. At the logic level, effective Boolean simplification could also allow lesser number of transistors to be used. Certain complex circuits such as the arithmetic logic unit (ALU), could be reused with multiplexers at the inputs to minimise duplication and prevent multi-access issues. Floor planning is another technique used whereby subcircuits with high level of interaction are placed next to each other to reduce the length of wire used which in turn would save some chip area.

Advanced packing techniques which are under the category of manufacturing are also used to reduce chip area. One key example is 3D integrated circuits where multiple integrated circuits are stack on top of one another to reduce the length of interconnects and the surface area [9]. However, limited interaction between each layer is advised for seamless operations. Furthermore, the number of layers stacked upon one another is also bound to manufacturing limitations and thermal constraints.

By physically shrinking the transistor size, the CMOS circuit could also become smaller. However, the gate width of the transistor directly affects the performance of a transistor [10]. A transistor with a wider gate has higher capacitance and could charge and discharge more quickly. Furthermore, they have much better noise margins and thus, are more reliable. The only downside of this is the larger size of the transistor. A way to overcome this issue is by only using transistors with narrower gate widths at parts of the circuit that do not require high performance and are non-critical. This approach would enable a reduction in chip area whilst not sacrificing too much performance.

4. Summary

In summary, various techniques have been developed to address the issue of power consumption and chip area optimisation. Each method has its own limitations and drawbacks. Furthermore, as transistors become smaller, there be a point where the transistor would no longer be able to be shrunken any further. This is due to electrons having a finite volume and the gate of the transistor could not be smaller than electron itself. Hence, new technologies needed to be developed in the future in order to create smaller and more powerful chips. Before such a

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bottleneck arises, there is still room for improvement for the current integrated circuits as it is not perfect yet. New materials could be used in the circuit level or even on the transistor to improve power consumption and potentially decrease chip area. Better layout schemes and software algorithms could also be used to pack the transistors as close as possible. However, all these theories and techniques could not be achieved without more precise and mature manufacturing process which deals with practical and physical limitations.

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