The Era of GAAFET Is About to Come

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ABSTRACT

In recent years, with the development of the semiconductor industry, Moore's Law has gradually become ineffective, making it increasingly difficult for people to improve chip manufacturing processes. Many people believe that Moore's Law will no longer exist. However, with Samsung announcing the production of 3-nanometer gate-all-around (GAA) architecture process technology chips on June 30, 2022, the chip process has been further advanced. Moore's Law is expected to continue in the coming years. This article will mainly introduce why GAAFET will become the mainstream field-effect transistor in the future. The potential problems that GAAFET may encounter in its future development will also be analyzed, including massive research and development costs and a longer research and development cycle.

Keywords: GAAFET, FinFET, Moore's Law, gate-all-around.

1. INTRODUCTION

Moore's Law was proposed by one of the founders of Intel, Gordon Moore, in April 1965. Its core content is that as the price remains unchanged, the number of accommodatable components on an integrated circuit will double approximately every 18-24 months, and the performance will double [1,2]. This trend has been ongoing for over half a century and is considered an observation or speculation rather than a physical or natural law. Before GAA, the semiconductor manufacturing process mainly consisted of two important eras: Planar FET and Fin Field Effect Transformer (FinFET). In the late 1950s, Bell Laboratories developed MOS tubes, officially ending the era of electronic tubes in computers. In the following 50 years, efforts were made to improve the Planar FET process to 20nm, and it was found that it was difficult to break through the bottleneck of the 20nm process. In 2000, Professor Hu Chenming from the University of California, Berkeley, introduced a new structure for field-effect transistors called FinFET. As the name implies, its structure resembles a fish [3]. FinFET has broken through the critical process node of 20 nm in the chip manufacturing process, and it has developed the chip process to below 5 nm in recent years. However, the current FinFET process can only develop to 2 nm and is still in the research and development stage [4]. Most people are not optimistic about increasing the process of FinFET to below 2nm. So, another high-performance structure, GAAFET, emerged, which is believed to replace FinFET and continue Moore's Law [5].

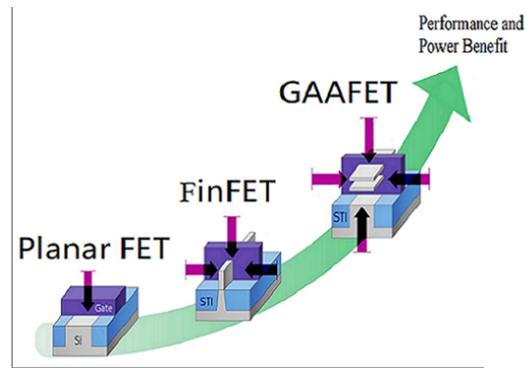


Fig. 1. FET development path and MBCFET structure [6].

Compared with the traditional FinFET, where only three sides of the channel are covered by the gate, in the case of GAAFET, if we take the example of a nanowire channel design, the entire outline of the channel is completely covered by the gate, indicating better control of the channel by the gate. You can see the specific structure of GAAFET in Fig.1. Currently, Samsung is developing 3nm GAAFET, which is expected to break through the 2nm chip manufacturing process in the future, replacing FinFET. In conclusion, GAAFET is the newest chip structure after FinFET.

2. MORE DETAILS ABOUT GAAFET

In this section, I will focus on introducing more details about GAAFET, including but not limited to its structure, production process, and advantages compared to FinFET. By introducing these contents, I want readers to better understand what GAAFET is and why it is expected to replace FinFET and continue Moore's Law.

2.1 *The Different Structures of GAAFET*

The GAAFET has two common structures: one is

the Nanowire GAAFET (NW GAAFET), which uses nanowires as the fin of the transistor, and the other is the Multi-Bridge-Channel FET (MBCFET), which appears in the form of nanosheets. Both of these structures can achieve a 3nm process node. Firstly, the following is about NW GAAFET.

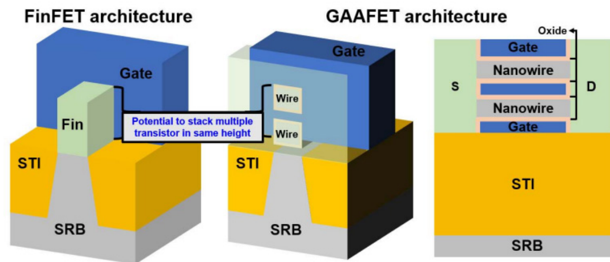


Fig. 2. Structure comparison between FinFETs and NW GAAFETs (Not to scale) [7].

In Fig. 2, we can visually see the structural differences between FINFET and NW GAAFET. In traditional FinFET, the channel is only surrounded by the gate on three sides, while in NW GAAFET, the entire outline is completely enveloped by the gate. This means that the gate has better control performance over the channel. What's more, compared to FinFET structures, GAAFET demonstrates the possibility of integrating more devices with the same height [7]. GAAFET architecture can achieve more functional units within a given chip area by vertically integrating multiple transistors, improving chip performance and density.

As for MBCFET, we can also refer to it as Nanosheet GAAFET (NS GAAFET). The difference lies in the fact that the channel of NW GAAFET is composed of nanowires, while the channel of NS GAAFET is composed of nanosheets. The transition from GAAFET to MBCFET can be seen as a leap from two-dimensional to three-dimensional. As shown in Fig. 3, compared to NW GAAFET, MBCFET has a wider total channel width and a more complex manufacturing process.

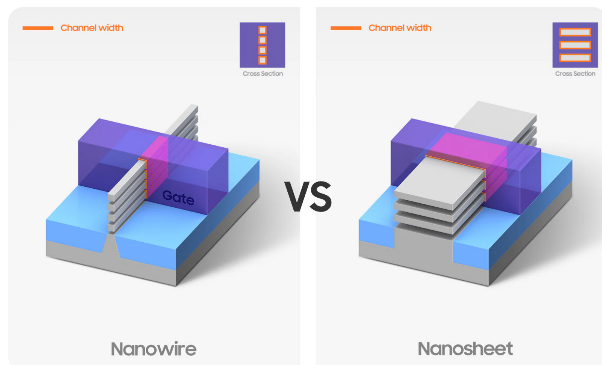


Fig. 3. Nanowire and NanoSheet structure [8].

Based on NW GAAFET, many scholars and engineers in the semiconductor industry have also designed different structures. For example, Yi-Wen Lin and his research team from the Department of Engineering and System Science at National Tsing Hua University proposed Tightly Stacked 3D Diamond-Shaped Ge Nanowire Gate-All-Around FETs in 2021[9]. As shown in Fig. 4, the channels of GAAFET are made into stacked diamond shapes. The channel material is also replaced with germanium, which allows the four sides of the channels to contact the gate and strengthens the control ability of the gate to the channel. The tight stacking of germanium nanowires makes them more stable and less prone to bending or collapsing during manufacturing. At the same time, this device is highly compatible with current technology platforms, so it has very good application prospects.

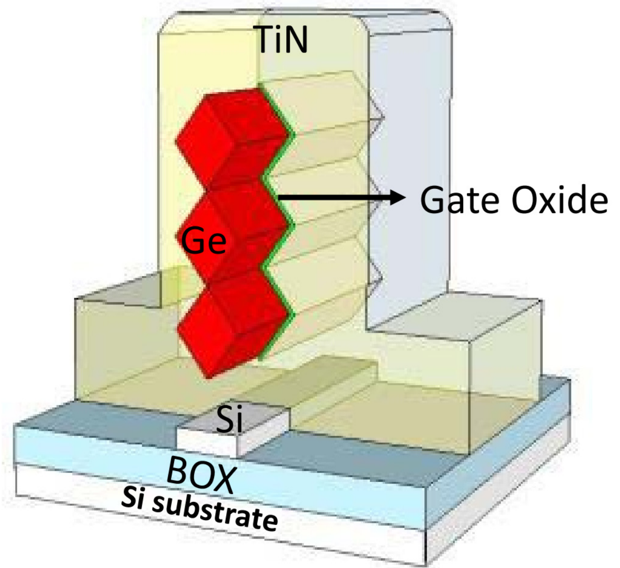


Fig. 4 Structure diagram of tightly stacked diamond-shaped Ge-NW GAAFET [9].

Upon reaching this point, some doubts may arise. Will the performance of NW GAAFET be improved by dividing its nanosheets single stack into nanosheets double stack to increase the contact area between the channel and gate? Theoretically, this would be valid. However, in reality, this is not the case. Here, we are going to introduce the concept of channel effective width. As shown in Fig. 5, scientists have found that dividing a single stack into a double stack and still aiming for 1.3 times the effective width (Weff) will inevitably increase the total width of the channels, thereby increasing the overall circuit area, which is undesirable in IC design. Therefore, the nanosheets single stack GAAFET is currently the most promising structure with the highest potential to replace FinFET in the future [10].

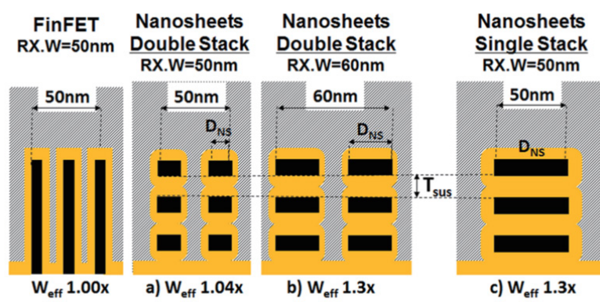


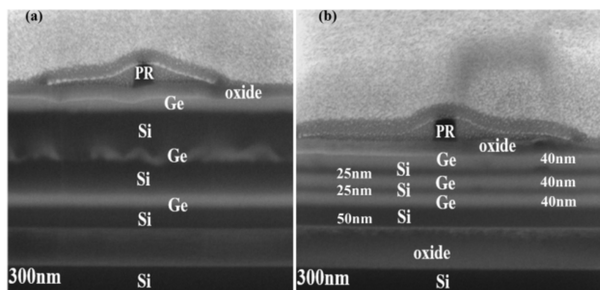
Fig.5 The structure diagrams of FinFET, nanosheets single stack GAAFET, and nanosheets double stack GAAFET [10].

In the various structures of NW GAAFET and NS GAAFET mentioned above, we can see that scientists and engineers not only pursue performance but also consider process stability and feasibility, overall device area, and the potential development of the device in the future semiconductor industry.

2.2 *The manufacturing process of GAAFET*

In this section, I will focus on introducing the mainstream manufacturing process of GAAFET in the current semiconductor industry - Ge Nanosheets GAAFET Fabricated by 2D Ge/Si Multilayer Epitaxy, Ge/Si Selective Etching, to give readers a preliminary understanding of the specific manufacturing process of GAAFET and the technical difficulties it may encounter during the manufacturing process.

The specific manufacturing process of Ge NS GAAFET will be introduced first. The initial step is to grow silicon/germanium epitaxial multilayers on the substrate using low-pressure chemical vapor deposition. Because of the good etching selectivity of Ge/Si epitaxial multilayers, Ge/Si epitaxial multilayers could be used as the starting material. Island mode and two-dimensional (2D) mode are now the primary growth modes of silicon/germanium epitaxial layers. As shown in Fig. 6(b), the epitaxial layers grown in 2D mode are flatter and smoother, suitable for device manufacture [11]. Therefore, the current GAAFET process generally uses 2D mode to prepare silicon/germanium epitaxial layers.



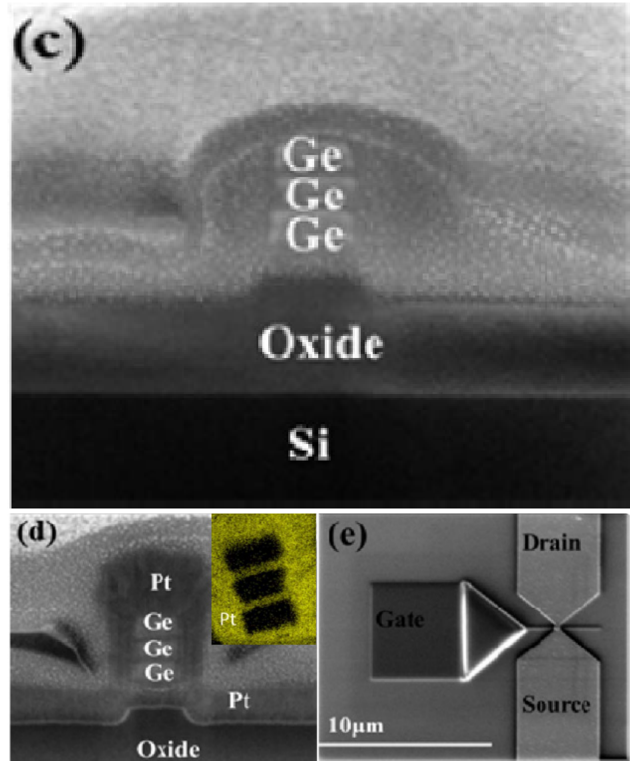


Fig.6 The cutaway views of Ge/Si epitaxial layers grown at two growth modes, (a) island mode and (b) 2D mode;

(c) The structure of the Stacked Ge nanosheet formed by the selective etching;

(d) The formation of gate dielectric and metal;

(e) A planform of a finished device [11].

After the growth of the silicon/germanium epitaxial multilayers is completed, electron beam lithography is used to define a fin for the channel, as well as the extension region of the source and drain, which is formed by a Cl_2/HBr-related etching process. Then, selective etching of silicon in the silicon/germanium epitaxial layers is carried out using the TMAH water solution at 60°C. Due to the significant lattice mismatch between silicon and germanium, the nanosheet dislocations are inevitable. Therefore, after the selective etching, the dislocations on the germanium nanosheets are removed by forming gas annealing, which also forms the stacked Ge nanosheet structures, as shown in Fig.6 (c).

Next is the gate's formation. Fig. 6 (d) shows that a high-k dielectric, Y_2O_3, is uniformly deposited around the stacked channel using atomic layer deposition, serving as the gate dielectric. Platinum is then directly and uniformly written onto the surface of Y_2O_3 as the gate metal using a focused ion beam. Finally, in the pMOSFET, a highly doped source and drain are formed by three-step ^{11}B ion implantations. As for the nMOSFET, three-step ^{31}P ion

implantations make a highly doped source and drain. The dopant activation and annealing for 11B and 31P are done through a two-step rapid thermal annealing process with two different temperatures that need precise control to ensure product quality. A complete GAAFET device is formed [11], as shown in Fig.6 (e).

Based on our preliminary understanding of the entire Ge NS GAAFET manufacturing process, we can easily conclude that temperature control is a big challenge in the manufacturing process of GAAFET, which directly affects the selective etching effect of TMAH aqueous solution, the removal effect of dislocations by FGA, the effect of annealing after ion implantation on repairing lattice damage and activating dopant and some other aspects of the GAAFET manufacturing process. What's more, lithography technology and ion implantation technology are challenges that must be overcome in GAAFET manufacturing. The development of lithography technology greatly helps break through the technological nodes in chip manufacturing and reduce chip manufacturing costs. Meanwhile, the uniformity and accuracy of ion implantation can effectively improve the yield of GAAFET products and the performance of the devices themselves.

2.3 *Advantages of GAAFET over FinFET*

GAAFET is expected to replace FinFET and continue Moore's Law from multiple aspects.

First of all, in terms of device performance, due to the two-dimensional to three-dimensional leap achieved by the contact between the channel and gate of GAAFET, it is easy to see that the control capability of GAAFET gate over the channel is stronger than that of FinFET. Therefore, generally speaking, GAAFET has lower power consumption than FinFET. Furthermore, regarding AC frequency performance, when the nanosheet design has wider and thinner wires, due to the better trade-off between effective current and effective capacitance, NS GAAFET performs better than FinFET[10]. As shown in Fig. 7, FinFET performs better in AC frequency performance than traditional square NW GAAFET but is lower than NS GAAFET.

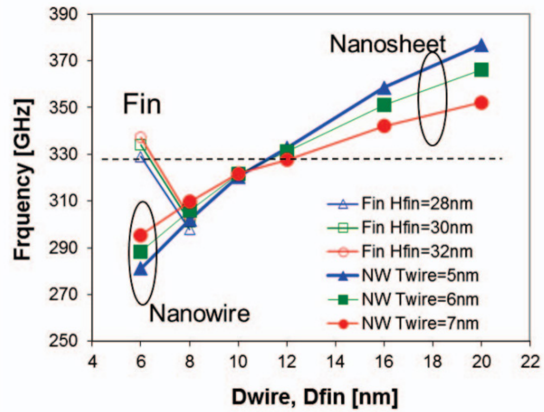


Fig.7. AC frequency performance comparison between FinFET and 2-stack nanowires as a function of D_{fin} or D_{wire}. Wider and thinner nanosheets perform better than FinFET, while conventional square-type NW shows lower performance[12].

Next is the advantage of NS GAAFET in terms of device area. We introduced the concept of W_{eff} in section 2.1 but only compared nanosheets single stack GAAFET and nanosheets double stack GAAFET - under the assumption of a certain stack/pitch height and fixed stack/pitch spacing, achieving the same W_{eff}, NS single stack GAAFET occupies a smaller area. Compared to FinFET, we can utilize wider, thinner, and stacked wire structures to make NS GAAFET match or surpass FinFET in terms of area performance [12]. Therefore, it can be concluded that NS GAAFET has greater potential in reducing device area compared to FinFET.

GAAFET has scalability in terms of power consumption, AC frequency performance, and device area and good scalability in terms of resistance to thermal effects and electron migration. GAAFET operates at a low power state in most environments, generating less heat. Its structure, with a fully surrounding gate, allows for better heat dissipation and reduces the impact of thermal effects on device performance. Therefore, GAAFET can provide better resistance to thermal effects. Moreover, by fully surrounding the channel material with the gate, GAAFET improves its control over electrons in the channel, reducing leakage current and hindering electron migration, thus reducing power consumption. Therefore, GAAFET also exhibits good scalability in electron migration resistance.

3. FUTURE & CHALLENGE

Through the analysis of GAAFET above, we can conclude that GAAFET will be the absolute leading technology in the semiconductor industry in the next few years.

Its development potential in low-process technology is sufficient to replace FinFET and continue Moore's Law.

Although GAAFET has many advantages compared to the currently mainstream FinFET, its development has been very slow due to its more complex structure, stricter material requirements, and the incompatibility of GAAFET's design and manufacturing processes with current technology platforms. Only a few large companies, such as TSMC and Samsung, can produce GAAFET with low-process technology. On June 17, 2022, TSMC unveiled its next-generation advanced process technology, N2, which refers to 2nm, at the 2022 Technology Symposium, and it is expected to enter mass production by 2025. Regarding microstructure, N2 adopts Nanosheet (GAAFET) instead of FinFET [13]. On the 30th of the same month, Samsung announced the start of production for its 3nm chips featuring the GAAFET architecture [1]. Currently, Samsung and TSMC are the only ones globally engaged in the research and development of GAAFET, while the market demand for low-process chips is enormous. For example, technology companies such as Apple and Intel that cannot independently produce low-process chips in the future need chips with stronger performance and smaller areas to improve their market competitiveness. To this day, the competition between TSMC and Samsung remains evenly matched, but if one side can achieve mass production of low-process GAAFET chips and achieve a significant leap in performance, this balance will be instantly broken, and a flood of orders from various tech companies will emerge.

In conclusion, the current research and development of GAAFET is still very challenging, which requires not only billions of dollars in investment but also the joint development of other fields, such as more advanced lithography machines, more compatible IC design platforms, and more complete production lines for low-process GAAFET chips, all of which are indispensable. Only through multi-field joint development can the final GAAFET production achieve high yield, good stability, and low manufacturing costs. Therefore, the research and development of low-process GAAFET faces a long and arduous journey.

4. CONCLUSION

In this paper, we introduced the content of Moore's Law and different structures of field-effect transistors and brought up GAAFET as the successor to FinFET to continue Moore's Law in the coming years. I also summarized more details about the structure and process of GAAFET and its advantages compared to FinFET, leading to the conclusion that the era of GAAFET is about to come. Similarly, we analyze the prospects of GAAFET and its potential challenges in future development.

Although only Samsung and TSMC are currently capable of manufacturing low-process GAAFET, its many advantages, such as high potential for device area reduction, low power consumption, and good device performance, determine that GAAFET will become the mainstream architecture for low-process chips in the coming years. Perhaps, like FinFET, it cannot continue Moore's Law for a long time but is destined to become an irreplaceable milestone in the development history of the semiconductor industry. The research and development path of GAAFET may be full of thorns, but we need to be down-to-earth and strive to achieve mass production of low-process chips as soon as possible to enter the era of GAAFET.

REFERENCES

[1] Samsung (2022). Samsung Begins Chip Production Using 3nm Process Technology With GAA Architecture. https://semiconductor.samsung.com/news-events/news/samsung-begins-chip-production-using-3nm-process-technology-with-gaa-architecture/?wcmmode=disabled.

[2] Moore, G. E. (1965). "Cramming more components onto integrated circuits." Electronics, 38(8), 114-117.

[3] D. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," in IEEE Transactions on Electron Devices, vol. 47, no. 12, pp. 2320-2325, Dec. 2000, doi: 10.1109/16.887014.

[4] V. P. -H. Hu, P. -C. Chiu, A. B. Sachid and C. Hu, "Negative capacitance enables FinFET and FDSOI scaling to 2 nm node," 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2017, pp. 23.1.1-23.1.4, doi: 10.1109/IEDM.2017.8268443.

[5] Chander Mohan1, Sumit Choudhary2, B. Prasad3, "Gate All Around FET: An Alternative of FinFET for Future Technology Nodes," International Journal of Advance Research in Science & Engineering, pp 561-569, Vol6, July 2017

[6] Zhang, S. (2020) Review of Modern Field Effect Transistor Technologies for Scaling. In:2nd International Conference on Electronic Engineering and Informatics. Lanzhou.

[7] C. -C. Lee, P. -C. Huang and T. -P. Hsiang, "Interactive Lattice and Process-Stress Responses in the Sub-7 nm Germanium-Based Three-Dimensional Transistor Architecture of FinFET and Nanowire GAAFET," in IEEE Transactions on Electron Devices, vol. 69, no. 12, pp. 6552-6560, Dec. 2022, doi: 10.1109/TED.2022.3216227.

[8] Samsung (2022). Find the optimal for the best. Part 1. https://semiconductor.samsung.com/news-events/tech-blog/gaa-dtco-for-ppa/

[9] Y. -W. Lin et al., "Tightly Stacked 3D Diamond-Shaped Ge

Nanowire Gate-All-Around FETs With Superior nFET and pFET Performance," in IEEE Electron Device Letters, vol. 42, no. 12, pp. 1727-1730, Dec. 2021, doi: 10.1109/LED.2021.3125059.
[10] N. Loubet et al., "Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET," 2017 Symposium on VLSI Technology, Kyoto, Japan, 2017, pp. T230-T231, doi: 10.23919/VLSIT.2017.7998183.
[11] C. -L. Chu et al., "Stacked Ge-Nanosheet GAAFETs Fabricated by Ge/Si Multilayer Epitaxy," in IEEE Electron Device Letters, vol. 39, no. 8, pp. 1133-1136, Aug. 2018, doi: 10.1109/LED.2018.2850366.
[12] S. -D. Kim, M. Guillorn, I. Lauer, P. Oldiges, T. Hook and M. -H. Na, "Performance trade-offs in FinFET and gate-all-around device architectures for 7nm-node and beyond," 2015 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Rohnert Park, CA, USA, 2015, pp. 1-3, doi: 10.1109/S3S.2015.7333521.
[13] Wannan (2022). End FinFET transistors! TSMC officially announced a 2nm power consumption reduction of 30%. https://news.mydrivers.com/1/839/839766.htm