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Research on Latch-up effect suppression method of IC based on CMOS technology

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Abstract:

Latch-up effect is a kind of parasitic effect in CMOS integrated circuits. Taking CMOS inverter as an example, this paper analyzes the formation mechanism of latch-up effect in CMOS integrated circuits, deduces the trigger conditions of latch-up effect by establishing equivalent circuit models, introduces the methods of suppressing latch-up effect from layout design and process optimization, and finally conducts simulation test to verify the effect of suppression methods.

Keywords: CMOS integrated circuit, latch-up effect, suppression methods, layout design, process optimization

1. Introduction

Complementary Metal Oxide Semiconductor (CMOS) integrated circuit is the core of modern electronic technology, but also digital and analog circuit design, radio frequency communication, sensors and other fields essential circuit structure, with other circuits can not match the advantages of low power consumption. However, the inherent latch-up effect in CMOS structure will seriously affect the effect of the circuit or even damage the circuit. With the continuous development and improvement of nanotechnology, the device size continues to shrink, and the problem becomes more prominent[1,2], to a large extent, hinders the improvement of circuit system performance and integration. The emergence of new processes will solve this problem by providing a reliable solution. This paper will study the suppression method of latch-up effect based on CMOS technology, which can lay a foundation for the wide application of integrated circuit in the fields of communication, medical equipment and microprocessor.

2. The Basic Pprinciple of Latch-up Effect

2.1 *Mechanism of Latch-up Effect*

The parasitic bipolar transistors inside CMOS devices interact with each other, causing them to be triggered at the same time, and forming a low impedance high current channel between the power source and the ground, which is the latch-up effect[1]. This paper will take CMOS inverter as an example to explore the formation mechanism of latch-up effect.

Figure 1 shows a cross-section of the N-well CMOS inverter structure with a parasitic bipolar transistor. It can be seen from the figure that the CMOS inverter structure has longitudinal PNP and transverse NPN transistors coupled through an N-well and a common substrate, and the base region of the transistor is connected to a non-zero parasitic resistance between the power supply and the ground terminal.

The generation of latch-up effect mainly involves the N-P-N-P structure composed of two transistors. Figure 2 shows the further simplified and equivalent CMOS inverter structure. When the collector current of one transistor rises sharply to the critical value due to the impulse voltage or impulse current, its emitter junction is forward biased, and the current flows into the other transistor, forming a positive feedback loop to trigger the latch-up. If current flows into node X, rises, then of Q2 increases, causing to decrease. The decrease of will lead to the increase of , resulting in a further increase of . If the loop gain is greater than 1, the cycle continues until both transistors are fully switched on, creating a very large conduction current between the power source and the ground, and the circuit generates the latch-up[3].

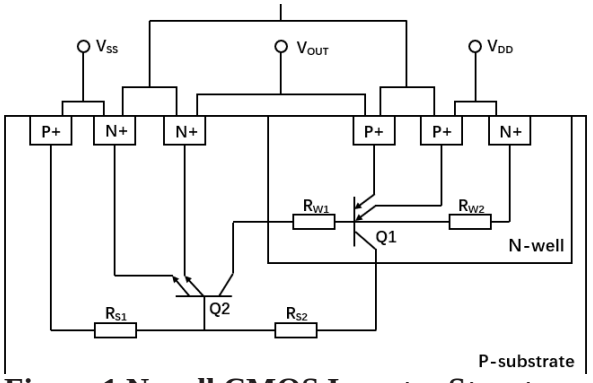

Figure 1 N-well CMOS Inverter Structure Profile

The root cause of the latch-up effect is the simultaneous conduction of the two parasitic tubes, which is the result of the positive bias of the parasitic tube emitter junction caused by the voltage drop generated by the displacement current in the parasitic resistance. The displacement current can be generated by the impulse voltage, or it can be caused by noise in the substrate and well. When a positive impulse voltage is applied at the output pin position, there will be holes diffused into the well, and the holes will enter the substrate when the reverse bias voltage between the well and the substrate is applied. The majority carrier current creates a voltage drop in the substrate resistance, and when the voltage drop is large enough, the parasitic NPN tube emitter junction will be forward biased. Similarly, if a negative impulse voltage is applied, the electron flow will flow into the well causing a latch-up effect[5].

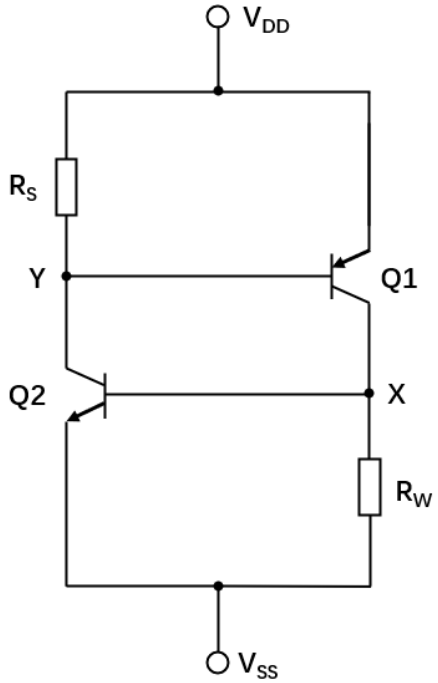

Figure 2. Simplified CMOS Inverter Structure Model

2.2 *Trigger Conditions of Latch-up*

The triggering conditions of the latch-up are derived from Figure 2: the emitter current gain of PNP tube Q1 is , the emitter current gain of NPN tube Q2 is , the well current is , the substrate current is , and the current flowing into point X is . According to the transistor's current relationship:

After sorting out the formulas, we can get:

and are small and can be neglected:

If , then . Such two transistors at the same time form a positive feedback, that is, a low impedance loop, so that the parasitic transistors maintain the on-state, gushing a heavy current to the ground from the power supply, and make the voltage between the power supply and the ground greatly decreased, resulting in a latch-up effect.

In summary, the three basic conditions for triggering the latch-up effect can be obtained:

(1)Loop gain ;

(2)The emitter junction of both transverse NPN and longitudinal PNP transistors is forward biased;

(3)The maximum current emitted by the power supply is greater than the maintenance current required for parasitic transistor conduction[4].

3. Suppression Method of Latch-up Effect

According to the above conditions, it is easy to know that as long as any of the above conditions are destroyed, the latch-up effect can be effectively suppressed. This paper will introduce the method of suppressing latch-up from layout design and process optimization.

3.1 *Layout Design*

3.1.1 *Add Guarding Ring*

By adding N+ ring in the N-well and P+ ring in the P-substrate, the bypass resistors and in the emitter region are decreasing. The bias voltage and current gain of the parasitic transistor are reduced. Before the minority carriers are absorbed by the reverse-biased junction as majority carriers flow into the well, the minority carriers will be guided to the Guarding Ring instead of the base of the transistor, thus blocking the parasitic connection. At the same time, the flow of electrons is directed to the Guarding Ring of the substrate, the voltage near the boundary of the well is reduced, and the parasitic tube in the well is channeled. The Guarding Ring of majority carriers minimizes the voltage between the substrate and the well boundary through the majority carrier current, and suppresses the parasitic tube conduction in the well[5]. When the latch-up current tries to flow through these rings, they are quickly directed to the ground or power supply, cutting

off the path that triggers the latch-up effect, preventing the two parasitic bipolar tubes from conducting at the same time, thus avoiding the accumulation of current in the sensitive area, so as to prevent the latch-up effect, in addition to reducing the parasitic transistor current gain and the resistance of the block in the substrate, reducing the injection of minority carriers into the well and the probability of triggering the latch-up on the substrate. The Guarding Ring should be as close as possible to the power supply to reduce base resistance and isolate sensitive areas susceptible to latch-up.

3.1.2 *Reasonable Layout*

According to the trigger conditions, it can be seen that reducing the well resistance and substrate resistance can weaken the latch-up effect.

(1)By increasing the distance between NMOS and PMOS, a link in the current cycle can be destroyed, which makes the base region of the side NPN transistor thicker, so that the collection of carriers becomes more difficult and it is difficult to amplify the current.

(2)Annular winding is used in the part of the substrate potential connection, which can reduce the well resistance and substrate resistance, prevent the base and collector of the transistor from becoming equal electric potential, and destroy the on-condition.

(3)Ensure that the substrate contact and the well contact are close to the source end, which can shorten the resistance length of the well and the substrate and reduce its resistance value.

(4)In the design and use process, ensure that the input or output voltage does not exceed the absolute maximum rating of the chip to avoid the latch-up effect caused by too high voltage.

(5)Sufficient spacing should be maintained between the power line and the ground wire to reduce the possibility of the feedback path caused by the mutual influence of the two parasitic transistors. Thicken the power line and ground wire to reduce the series resistance and reduce the transverse current density.

3.2 *Process Optimization*

3.2.1 *Epitaxial Substrate Technology*

Epitaxial substrate technology reduces the current gain of parasitic resistance , and NPN tubes by epitaxially laying a low-doped silicon epitaxial layer on a heavily doped silicon substrate. The low doping properties of the epitaxial layer provide a high conduction path for the current and reduce the body resistance, thus reducing the voltage drop of the current on the well resistance and avoiding latch-up.

3.2.2 *Retrograde Well Technology*

Retrograde well technology can inject a high concentration of high energy impurity ions at the bottom of the well, so that the doping concentration of the well at the bottom to achieve the maximum, while the surface concentration is relatively low. This structure is called the retrograde well. In the retrograde well structure, after the electrons or holes reach the base, the high concentration of doping can effectively increase the recombination probability and prevent the electrons or holes from reaching the collector, thereby reducing the current gain of the transistor and avoiding the biased transistor to trigger the latch-up. The inverse doping well technique can not only suppress the latch-up effect, but also improve the stability and reliability of integrated circuits.

3.2.3 *Trench Isolation Technology and Silicon-on-Insulator Technology*

The trench isolation technology reduces the gain of the transverse transistor by creating an insulating tank between the PN junction. The ditch groove is composed of a shallow and a deep two-stage groove, which can weaken the path that may be formed between the two transistors, shorten the transverse spacing of the two transistors, isolate carriers, and completely cut off the circuit that may form a latch-up. The depth of the groove is proportional to the suppressive effect of the latch-up, saving the layout area and circuit cost.

Silicon-on-Insulator (SOI) technology is the most effective scheme to eliminate the latch-up effect. SOI introduces a layer of insulation between the silicon layer and the substrate. The insulation layer separates the device from the substrate, thereby preventing the formation of parasitic bipolar transistors. Due to the existence of the insulation layer, even if there is a parasitic capacitor between the devices, it will not form a PN junction that can be conducted, so the physical basis of the latch-up effect is eliminated. The isolation between devices is achieved through the insulation layer, rather than the traditional field oxidation isolation, that is, SOI technology also has the characteristics of all dielectric isolation, this isolation also reduces the parasitic capacitance and leakage current, thereby improving the response speed of the integrated circuit, reducing power consumption, and fundamentally avoiding the formation of latch-up[6].

The two are often used together to achieve more effective device isolation and improve integrated circuit performance.

3.2.4 *Fin Field-Effect Transistor Technology*

Fin Field-Effect Transistor (FinFET) technology can form a fin-like channel in three-dimensional space to improve

the performance of the transistor and reduce the probability of forming parasitic structures. The gate of the transistor controls the fish-fin shaped channel. This structure can effectively reduce the leakage current and enhance the ability of the transistor to control the current. In addition, the width of the FinFET transistor, the thickness of the shallow trench isolation and the transverse distance from NMOS to PMOS can be reduced by optimizing these structural changes, and the changes in the parasitic vertical and horizontal resistance can be reduced. In addition, it can reduce the sensitivity of FinFET devices to latch-up.

4. Test of the Suppression Effect of Latch-up

Taking the independent dual-well isolation layout used in combination with the layout design method and the trench isolation technology as an example, and using only the structural layout of the conventional Guarding Ring as a contrast, each pin of the two groups will be subjected to the sink/sourcing current stress test respectively to detect the voltage and current on the power supply to determine whether the latch-up is generated[8]. The profile diagram of the independent dual-well isolation layout is shown in Figure 3.

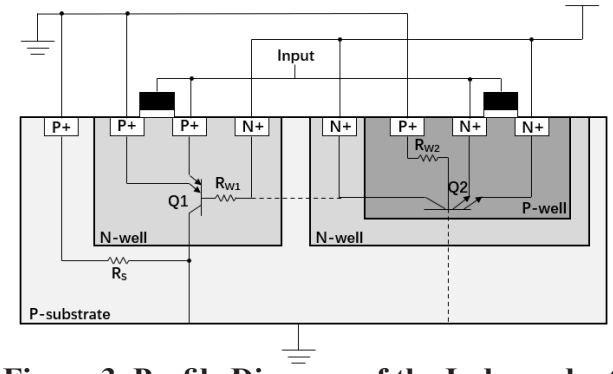

Figure 3. Profile Diagram of the Independent Dual-Well Isolation Layout

Set the sink/sourcing current 25~200mA, spacing 25mA, if the power supply current during the period is zero, the circuit is free of latch-up. If the power supply voltage drop is detected and accompanied by a certain margin of non-zero power supply current, the circuit generates the latch-up[7]. The latch-up test results are shown in Table 1. Compared with the test results, it is apparent that using the Guarding Ring structure alone for latch-up immunity is not ideal, but using the independent dual-well isolation layout can effectively prevent the latch-up effect.

Table 1 Comparison of Latch-up Test Data under the Two Layout Designs[7]

Pin Position	Sink/ Sourcing Current	Power Voltage Before Sink/ Sourcing	Power Current Before Sink/ Sourcing	Power Voltage After Sink/ Sourcing	Power Current After Sink/ Sourcing	Conclusion
	+0.025A	5.48V	0mA	1.44V	120mA	Latch-up
	-0.075A	5.48V	0mA	1.45V	120mA	Latch-up
	+0.075A	5.48V	41mA	1.49V	120mA	Latch-up
	-0.100A	5.48V	6mA	1.31V	120mA	Latch-up
	+0.200A	5.48V	0mA	5.48V	0mA	Latch-up Free
	-0.200A	5.48V	0mA	5.48V	0mA	Latch-up Free
	+0.200A	5.48V	0mA	5.48V	0mA	Latch-up Free
	-0.200A	5.48V	0mA	5.48V	0mA	Latch-up Free

Since CMOS devices will be affected by disturbance and other parasitic effects, especially thermal effects, thermal model or temperature compensation can be used in simulation. The test data can be corrected according to the results, and the parasitic effects can be ignored when the impact on the test results is small.

5. Summary and Prospect

Suppressing the latch-up effect of integrated circuits prioritizes the low cost layout aspect. Layout design is the most widely used method to suppress the latch-up effect of IC, but its suppression effect needs to be improved. The research and development of new technology can effectively improve the latch-up immunity, but it will bring high cost. Layout design and process optimization are often combined to obtain the best solution. There will be more effective and affordable methods in the future, and there is still a lot of research space available to suppress the latch-up effect.

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