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# Design of RF Communication Control Module Based on FPGA

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**Abstract:**

As society enters the era of the information explosion, the amount of information consumed per day has increased almost exponentially. At the same time, the corresponding transmission quality has also become higher and higher. These increasing indicators have promoted the continuous improvement of the standards of the carrier medium. At this stage, the vigorous development of the wireless communication field has brought about the rapid development of wireless communication technology, and technologies such as LTE and 5G have followed. While communication equipment continues to develop to solve the problems caused by the increase in the amount of information, more problems are constantly emerging: the wide variety of communication equipment causes great troubles for later maintenance and management; the imbalance of hardware resource allocation causes Too much waste of resources; more communication interference seriously affects communication quality... and many other problems. Therefore, the research on high-efficiency and high-performance wireless communication technologies and wireless communication systems is of great significance.

**Keywords:** FPGA, PCB, ISE, RF communication control module

## 1. Introduction

### 1.1 . *Purpose and meaning*

As the mobile Internet comes, the society enters the era of information bangs, the amount of information generated daily continuously expands, and the quality of transmission information is getting higher and higher. The transmission rate has gradually risen.

Nowadays, the field of wireless communication is thriving, and wireless communication technology is almost changing. Wireless communication technologies such as LTE, 5G have come successively. The limit of the spectrum resource application of the frequency band and the use of spectrum resources in high frequency bands are limited. Therefore, in order to obtain more spectrum resources and develop to a higher frequency band, it has become one of the primary choices.

### 1.2 . *Domestic and foreign research (application) situation and development trend related to this project*

In the 521-2002 standard of the IEEE protocol, the radio band of the 12-18GHz is called the K band, K is “K-Under”, referred to as KU band.

In the field of wireless communication, the KU band is widely used. In satellite communication, the KU band is a commonly used band. The main features are:

(1) The KU frequency band is wide, which can transmit various information and transmit a variety of services at the same time.

(2) The antenna diameter that receives the KU band is smaller than the size of other bands, and it is not easy to find.

(3) The impact of extreme weather such as rainfall on KU band satellite broadcast is more serious than other bands.

In the development of the KU band radio frequency communication system, Europe and the United States started earlier, and due to their components and process advantages in a leading position. Taking satellite communication as an example, relevant institutions in various countries have carried out research for many years, such as NASA in the United States, NASDA in Japan, ESA in Europe, ASI in Italy, etc. There are already many KU bands of military high -speed communication satellites. Its radio frequency sending channel, the instantaneous operating bandwidth has exceeded 1G, and at the same time, the linear output power of the miniaturized workmanship exceeds 100 watts.

### 1.3 . *Main work*

This article studies the design of the RF communication control module based on FPGA. The FPGA-based development platform is selected because FPGA has good programmable and configurable characteristics. The system configuration can be changed by directly modifying the software part of the design. This greatly enhances the

versatility of the hardware, realizes the reuse of hardware resources, saves on hardware costs, reduces the cost of subsequent maintenance, and makes the update and maintenance of the system easier to achieve. In hardware design, choosing a device that is more compatible with FPGA can reduce development costs. Therefore, the selection of each device is an important research objective. After comparing the performance of each device, the selection of each device is determined, and then the design of the schematic diagram and PCB packaging proceeds. Once the design of the hardware circuit is completed, the software test begins on the ISE platform using FPGA technology, and after debugging is completed, it is downloaded to the board.

# 2. Device selection and circuit design

## 2.1 . *System solution design*

The hardware part of the design scheme of this topic is as follows. FPGA can process data sent by the upper machine, and can also receive external data, such as faulty information, and fed back to the upper machine by FPGA.

## 2.2 . *FPGA selection*

In order to improve the universality and application scenarios of the hardware platform, it is hoped that the hardware platform is easier to update and maintain. This subject uses FPGA as the core to control the core of Xilinx's Spartan-3 series chips.

In the Spartan-3 series chips, Spartan-3A is applicable to applications that are more important than logic density. By comparing its technical characteristics, the following picture is the technical features of Spartan-3E chips and the technical features of Spartan-3 chips.

**Tbale 1 Technical features of Spartan-3E**

| Device | System Gates | Equivalent Logic Cells | CLB Array (One CLB = Four Slices) | | | | Distributed RAM bits(1) | Block RAM bits(1) | Dedicated Multipliers | DCMs | Maximum User I/O | Maximum Differential I/O Pairs |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Rows | Columns | Total CLBs | Total Slices | | | | | | |
| XC3S100E | 100K | 2,160 | 22 | 16 | 240 | 960 | 15K | 72K | 4 | 2 | 108 | 40 |
| XC3S250E | 250K | 5,508 | 34 | 26 | 612 | 2,448 | 38K | 216K | 12 | 4 | 172 | 68 |
| XC3S500E | 500K | 10,476 | 46 | 34 | 1,164 | 4,656 | 73K | 360K | 20 | 4 | 232 | 92 |
| XC3S1200E | 1200K | 19,512 | 60 | 46 | 2,168 | 8,672 | 136K | 504K | 28 | 8 | 304 | 124 |
| XC3S1600E | 1600K | 33,192 | 76 | 58 | 3,688 | 14,752 | 231K | 648K | 36 | 8 | 376 | 156 |

## 2.3 . *Selection of transceiver*

### 2.3.1 *Selection of RS-422*

In the selection of the transceiver, the RS-422 transceiver is selected. As the RS-422 transceiver, it is a communication interface with RS-422 as a communication standard. It has the characteristics of multi-nodes and Yiquang.com. It is widely used in the fields of instrumentation, security, transportation, industrial equipment and other fields. RS-422 is widely used in the industrial environment; in addition, the scenes of other application environments are more complicated. This often causes RS-422 to be greater interference in the actual application process. Therefore, it has more reliable and better performance devices to become the primary choice in a harsh environment.

### 2.3.2 . *Selection of RS-232*

In the case of achieving the same function, MAX3232E is more cost-effective. In terms of structure, the MAX3232E device consists of two circuit drives, two lines receivers, and a dual -charge pump circuit, which has a ± 15kV IEC ESD protective pins to the pin. Comply with the TIA / EIA-232-F standard. The charge pump and four small external capacitors are allowed to work under 3V to 5.5V power supply. These devices work at a data signaling rate of up to 250 kbit / s and the output pressure of the drive with a maximum 30V / μs drive. The MAX3232E circuit is mature and cost-effective, which can be used as the result of the selection of the RS-232 transceiver.

## 2.4 . *Selection of the level converter*

Before determining the selection of the level converter, choose the correct level conversion scheme. Today, most electronic systems generally need level conversion. The input voltage threshold and output voltage level of electronic equipment will vary, depending on the equipment technology and power supply voltage. To successfully connect the two devices, the following requirements must be met:

(1) The VOH of the driver must be greater than the VIH of the receiver.

(2) The VOL of the drive must be smaller than the VIL of the receiver.

(3) The output voltage of the drive must not exceed the I / O voltage tolerance of the receiver.

The 8 -bit dual -power voltage level conversion of the Texas Instrument (TI) converts SN74LVC8T245, SN74AVC8T245 provides higher design flexibility for the

hybrid I/O voltage in the conversion system.

### 2.5 . *Hardware circuit design*

The hardware circuit is mainly composed of FPGA chip, power module, level conversion module, buffer, interface circuit, transceiver, etc.

Because the principle of the FPGA chip is too large, it cannot be displayed here, so it only explains its working status. The external power supply voltage of FPGA is 5V. Since the FPGA chip needs 1.2V voltage to supply internal logic voltage (VCCINT), 2.5V is required to provide PLL analog voltage (VCCAUX), and IO voltage (VCCO_0/1/2/3) can be accessible 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V to provide different voltage standards for each area. Therefore, in terms of design, the 5V voltage of the external input is converted to 3.3V, 2.5V, 1.2V, etc. to maintain the normal work of FPGA chips. 3.3V is generally used to provide high levels of voltage and special function pins such as clocks, configuration circuits, and special function pins.

## 3. design of PCB

### 3.1 . *Basic layout*

In the layout of the PCB, you must first complete some basic design. The number of components should be arranged by the frame. Device, such as clock generators and crystal high -frequency devices, should be wrapped as much as possible when placing. After completing the preliminary design, the detailed layout after completion can be completed in accordance with the characteristics of the electronic devices used and its layout criteria.

#### 3.1.1 . *Layout Guidelines of THVD1452*

In order to prevent the phenomenon of surge transients that may occur in the industrial environment, external transient protection equipment is usually used to ensure the stability and reliability of the bus node design. Because these transients have a wide frequency bandwidth (from about 3 MHz to 300 MHz), high -frequency layout technology should be used during the PCB design period.

#### 3.1.2 . *Layout Guidelines of SN74LVC8T245*

(1) Winging electric containers should be used on the power supply.

(2) Short -line length should be used to avoid excessive loads.

(3) Putting the pads used for load capacitors or pull -up resistors on the signal path can help adjust the signal's rise and decrease time according to the system requirements.

#### 3.1.3 . *Layout Guidelines of FPGA*

(1) Filter capacitor and oscillator should be close to the power supply, and the front end of the oscillator should be placed.

(2) Add a resistor between the simulation ground (AGND) and the average place (GND), and the positive and negative simulation reference inputs should be filtered with capacitance (0.1UF).

(3) Try the cross -staggered wiring as much as possible to reduce signal interference.

(4) Clock crystal sources should be placed as close as possible to the FPGA clock special pins that are connected to it.

### 3.2 *Board of PCB*

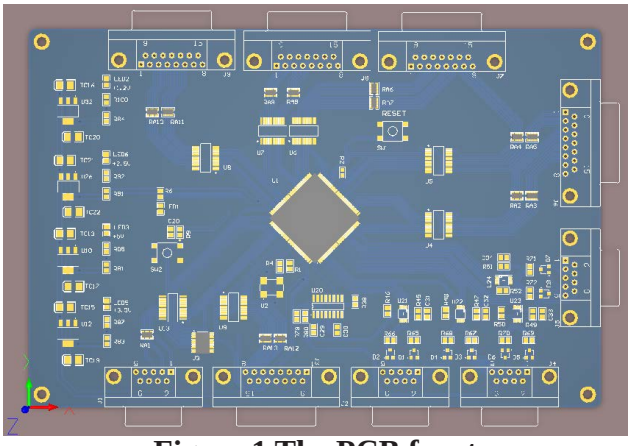

**Figure 1 The PCB front**

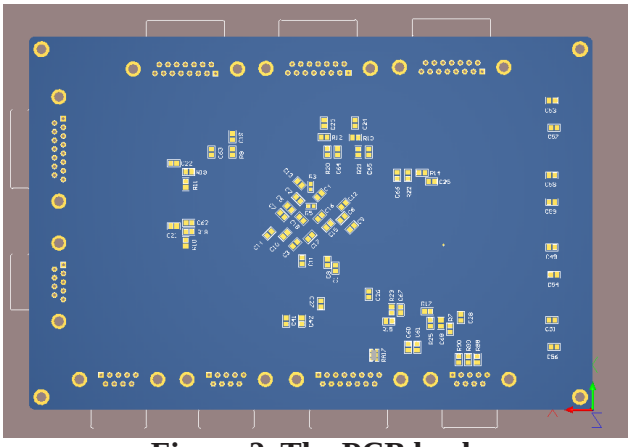

**Figure 2 The PCB back**

## 4. Debug

### 4.1 . *debugging of Hardware*

In order to prevent the circuit board from having a short circuit and a disconnection of electronic components, it is essential for hardware debugging. The hardware debugging is mainly to test whether the circuit board can supply normally, whether it will be short -circuit, and the interruption.

Use a multimeter to measure whether the power supply pins of FPGA, THVD1452, and MAX3232E are normal,

and then check whether the LED light can be turned on normally.

## 4.2 . *debugging of Software*

After the circuit board can be powered normally, whether the code to be carried out in the next step, whether the code can be recorded normally, it is mainly determined that the interface circuit can run normally. Records need to be tested by hardware. The main check -up part of the interface part is poor, whether the circuit has short circuit, and the circuit disconnection. After all the inspection is completed, the coded record is performed.

## 4.3 . *Functional implementation*

After the hardware debugging and software debugging are completed and the test is normal, some functions are completed on the circuit board. The main function is to complete the serial communication. If the circuit board can complete the serial communication with the upper machine and other devices, then the upper position can be achieved. The control of the radio frequency module of the circuit, that is, the FPGA receives the control information of the upper machine, and then converts the instructions to control other modules. In this way, the secondary conversion mainly determines whether the FPGA can communicate serialized with the upper machine normally.

### 4.3.1 . *Candidate communication and radio frequency module control*

Since there is no communication protocol between FPGA and the computer, in order to implement serial communication, you need to write another communication protocol. You can write code in accordance with UART's communication standards to implement communication protocols.

The transmission method is the RS-422 asynchronous serial. In order to ensure the normal transmission of the data, the data bit, starting bit, verification, etc. should be set.

The data bit is eight -bit data; the starting bit is before the data, which is triggered by the low level. When it is triggered, the data is transmitted; the verification bit is set to no verification.

Set the Potter rate after setting the data position, starting digit, verification digit, and stopping the bit. The serial port baud rate is 115200, and the internal clock in the FPGA is 100MHz, so the specified Potter rate is 115200/100MHz.

There are not many signals to process serial communication. There are system clocks, system reset, receiving RX, and sending TX. FPGA code design and design ideas are as follows: need to add a counter to ensure that the data is accepted.

First define the input signal, output signal, set the baud rate, and then define the main parameters of the sending module and receiving module; wire [7: 0] UART_DATA is a receiving data memory, which is used to store the received data until it is stored.

When controlling the 13-14GHz frequency signal, the upper machine and FPGA have realized 422 serial communication, so the upper machine can issue a command to control the FPGA to send instructions and send the decoction code; After receiving the command of the upper machine, FPGA will send the instruction and attenuation code to the transceiver, and then transmit the instruction information and attenuation code to the radio frequency module and attenuator, and then the RF module starts to receive the frequency signal; when there is no at the frequency of 13-14GHz, the radio frequency module will have no signal to be fed back to the FPGA by the transceiver THVD1452, and then the FPGA will be sent to the upper machine. The feedback does not have the frequency of 13-14GHz.

The process of receiving a 1-2GHz frequency signal is the same as 13-14GHz, but the sends attenuation code are less than 13-14GHz, so when receiving the 1-2GHz frequency signal, there is no need to connect an excess attenuator.

When controlling the sending 10-12GHz frequency signal, the upper machine and FPGA communicate through the serial port to realize the RS-422 communication, the upper machine sends a command, and control the FPGA sending instructions; After getting the command of the upper machine, then send the instruction to the transceiver, and then send the instruction to the radio frequency module. The radio frequency module determines whether the 10-12GHz frequency signal is sent according to the instruction. Then send it to the upper machine by FPGA to complete the information feedback.

In order to ensure that the radio frequency module can accurately receive instructions, the 422-interface communication protocol of the RF module needs to be defined. A complete data packet consists of the starting unit, the verification unit, and the command unit and the end unit.

(1) The starting unit is a byte length, which is the beginning of a complete command package. The 16 -bit inlet number is 0x7E in the fixed position.

(2) The end of the unit is a byte length, which is the beginning of a complete command package. The number of 16 -bit inlet is 0x7F.

(3) The verification unit adopts a 16 CRC verification polynomial to generate a 2 -byte CRC verification.

(4) Data transmission adopts asynchronous half -work communication method, 8 data bit, one stop bit, no school test, and the baud rate is 19200bps.

(5) The command unit consists of two parts: command control head and command body. The command control header is composed of module address, command number,

response sign, and command body length.
Use two bytes to represent the module address, the first byte is functional, and the second byte is the address coding.

**Table 2 Module function code**

| Module function | code |
|---|---|
| Attenuator | 0x01 |
| Frequency selection module | 0x02 |
| Time control module | 0x03 |
| If you need to add coding, you can add other codes according to actual needs. | |

**Table 3 Module address coding**

| Bit number | code |
|---|---|
| bit3up | 0 |
| bit3down | 1 |
| bit2---0 | Module code |

**Table 4 Command number**

| Command number | function |
|---|---|
| 0x10 | Set the module address |
| 0x11 | Settings |
| 0x12 | Set frequency |

**Table 5 Response sign**

| code | function |
|---|---|
| 0x00 | successful |
| 0x05 | wrong |
| 0x06 | Command data wrong |
| 0x07 | failed |

## 5. Summary

This project has completed the hardware control part of the KU band wireless communication system. Using the good characteristics of FPGA, the FPGA -based radio frequency communication control module design is designed; Type, selection of transceiver, selection of level converters, etc. This article is as follows:
(1) After referring to the parameters of the Spartan-3E series chip, the selection of the subsequent devices is more targeted. It mainly consider whether the configuration voltage meets, whether the logical output voltage matches, whether the device characteristics meet the working environment, whether the device price is in the Considering the scope, whether the device circuit is mature, etc., the more targeted selection not only has a clear direction of hardware circuit design, but also reduces design errors and simplifies the design.
(2) The design of the PCB is designed strictly according to the layout standards in the data manual. The setting of its standards mainly considers some interference of the device in the working environment, such as noise current, effective passing inductance, transient, surge of waves, waves surging Instant change, etc., these factors also

largely determine the length of the wiring. The position of the protection circuit is placed. According to the direction of the signal path, the position of the load capacitor capacitance is placed.

(3) The final debugging part is to check whether the circuit board can work properly. The debugging software debugging mainly depends on whether the code can be recorded normally and verify that the function controlled by the RF module can be realized.

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